

COMPAL CONFIDENTIAL

MODEL NAME : CDP70  
PCB NO : LA-E141P  
BOM P/N :  
GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge 14 UMA

Kabylake H


2016-07-01

REV : 0.2 (X01)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESD Component
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- XDP@ : XDP Component
- CONN@ : Connector Component

MB PCB	
Part Number	Description
DAB0001R000	PCB 1SC LA-E141P REV0 MB UMA 1

Layout Dell logo

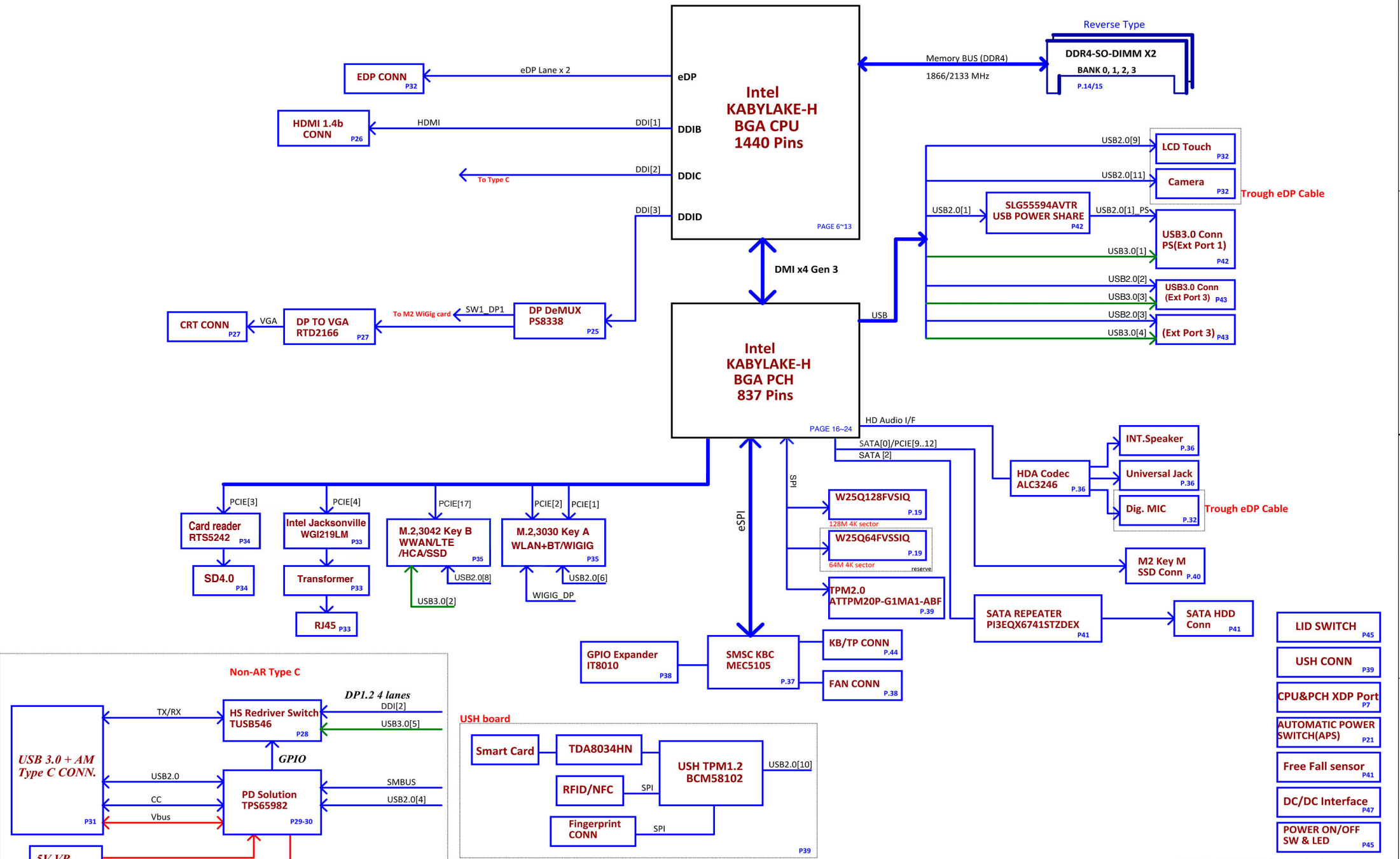


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PWB: K6NHT

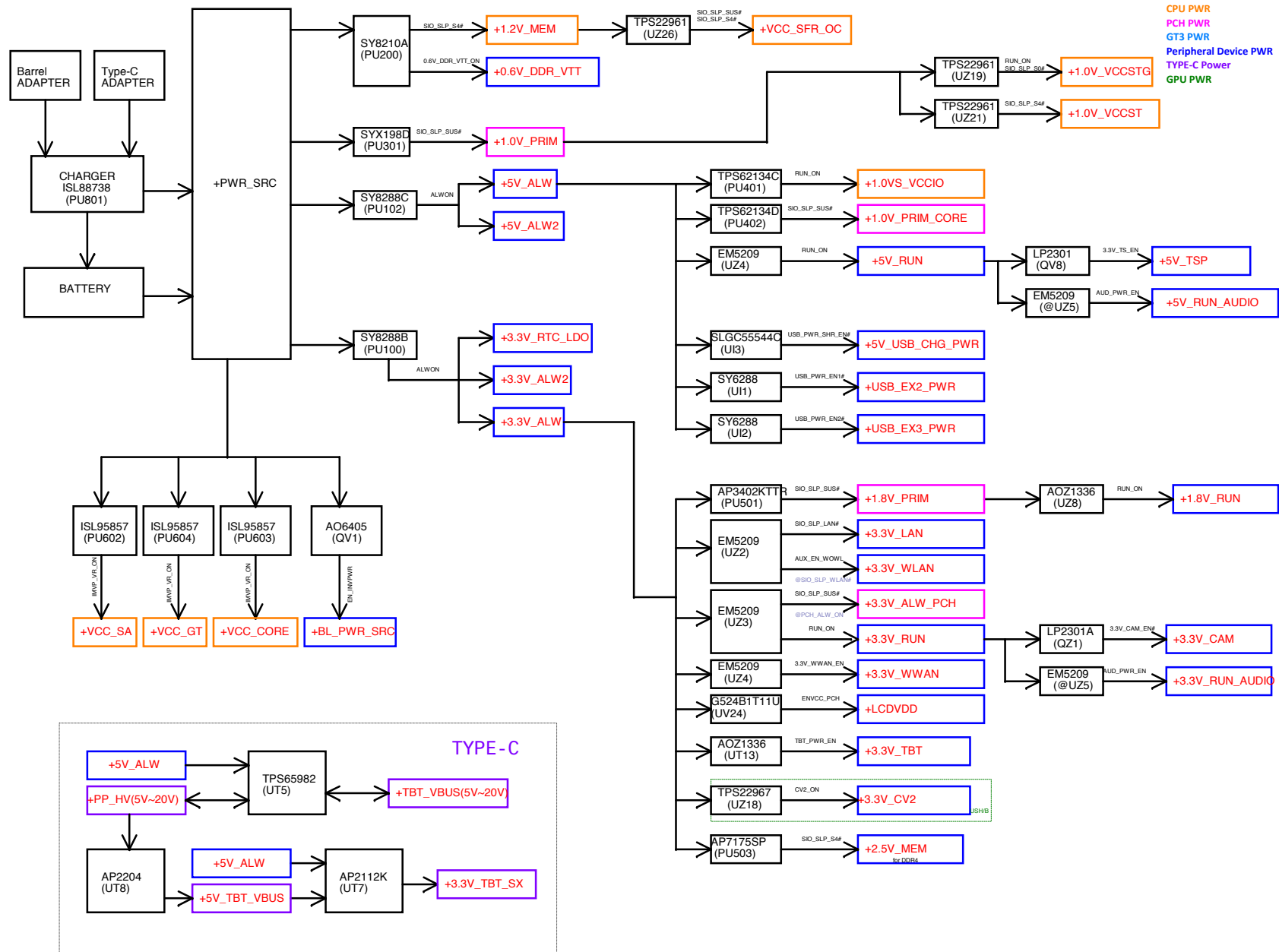
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A		LA-E141P		0.2	
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Breckenridge 14 UMA non-TBT Block Diagram







CPU PWR  
PCH PWR  
GT3 PWR  
Peripheral Device PWR  
TYPE-C Power  
GPU PWR

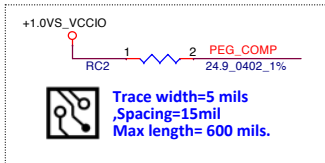
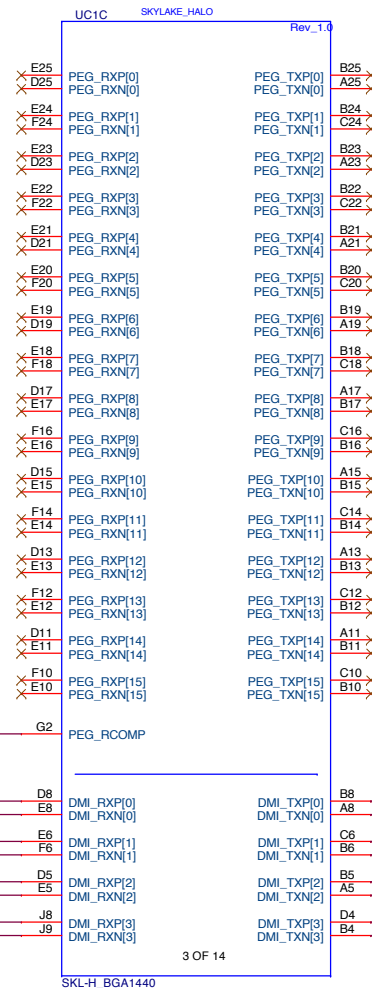
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Power Rails

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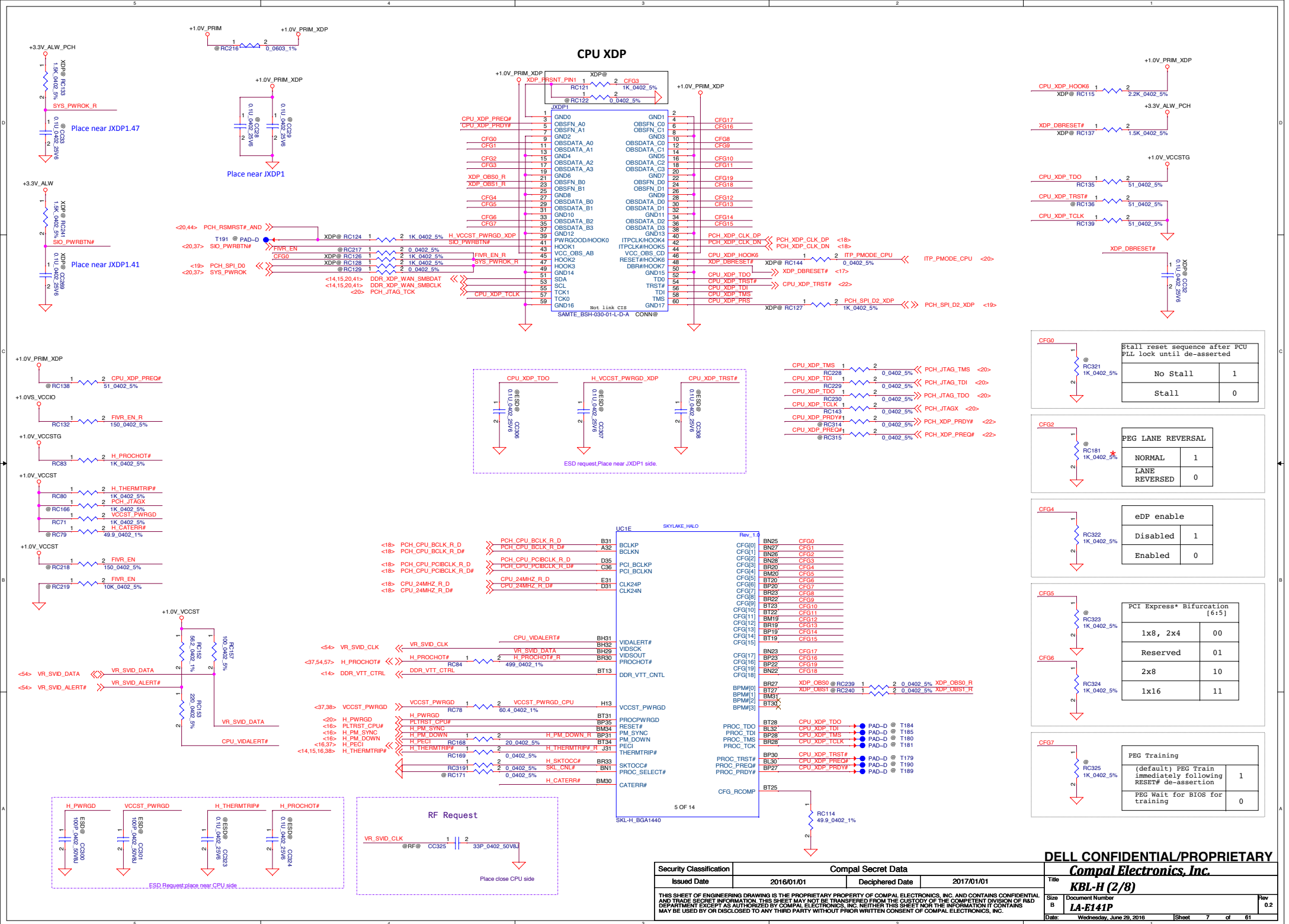
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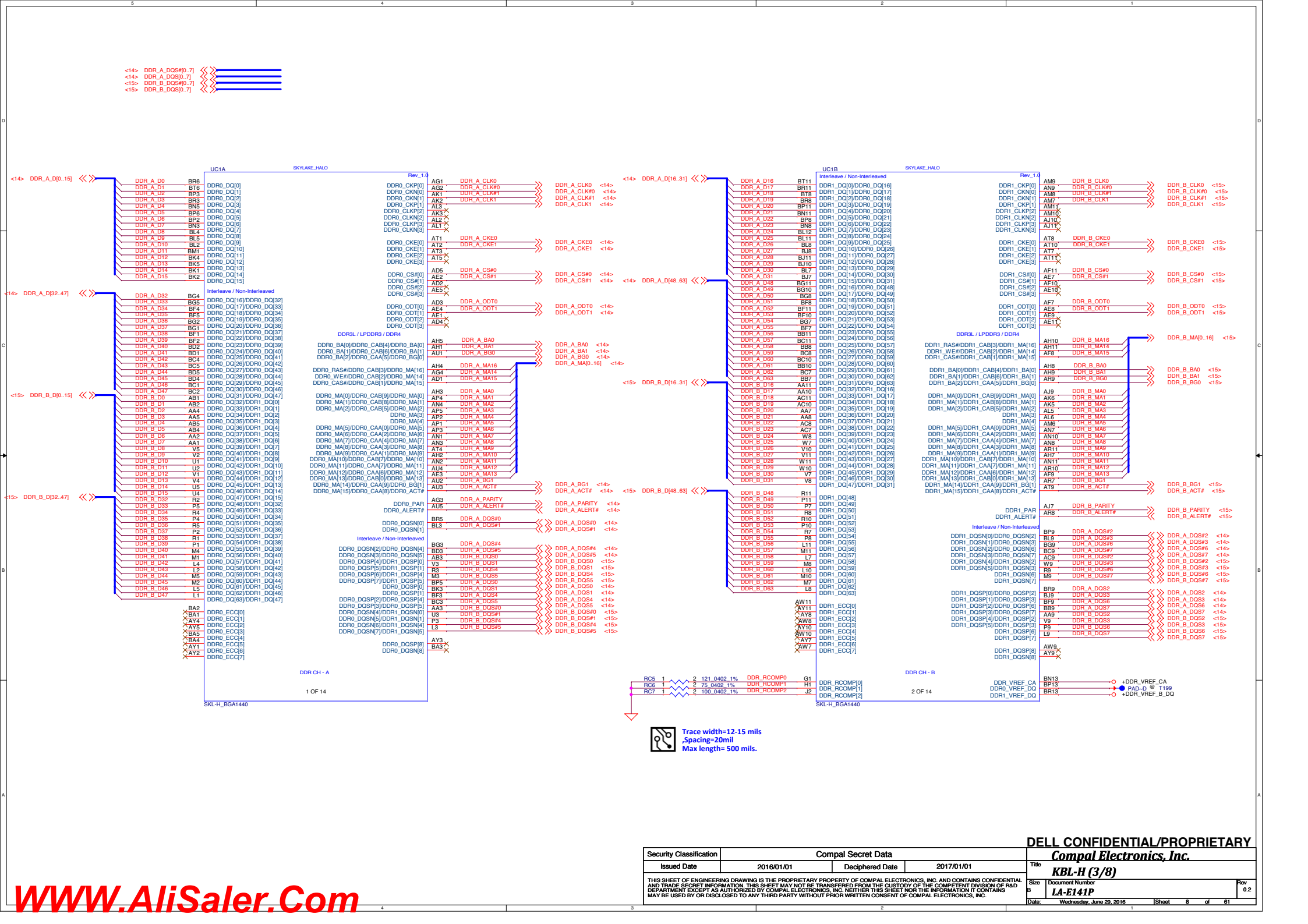
Size A Document Number LA-E141P Rev 0.2

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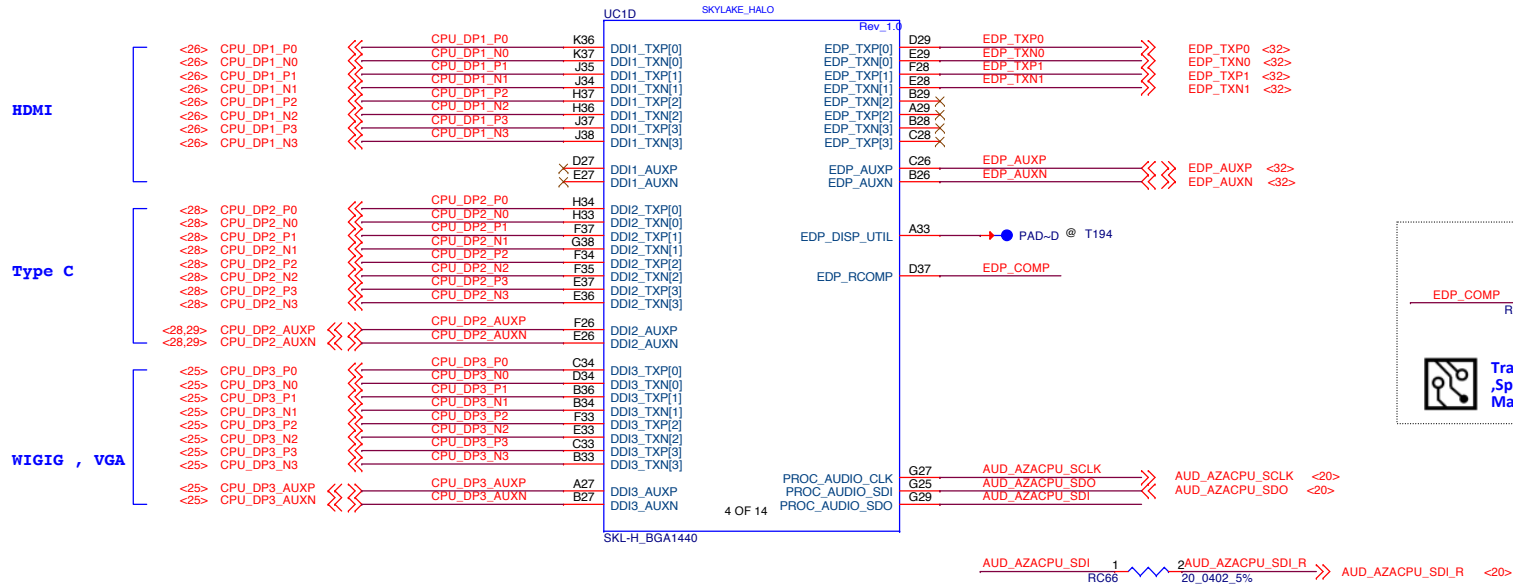
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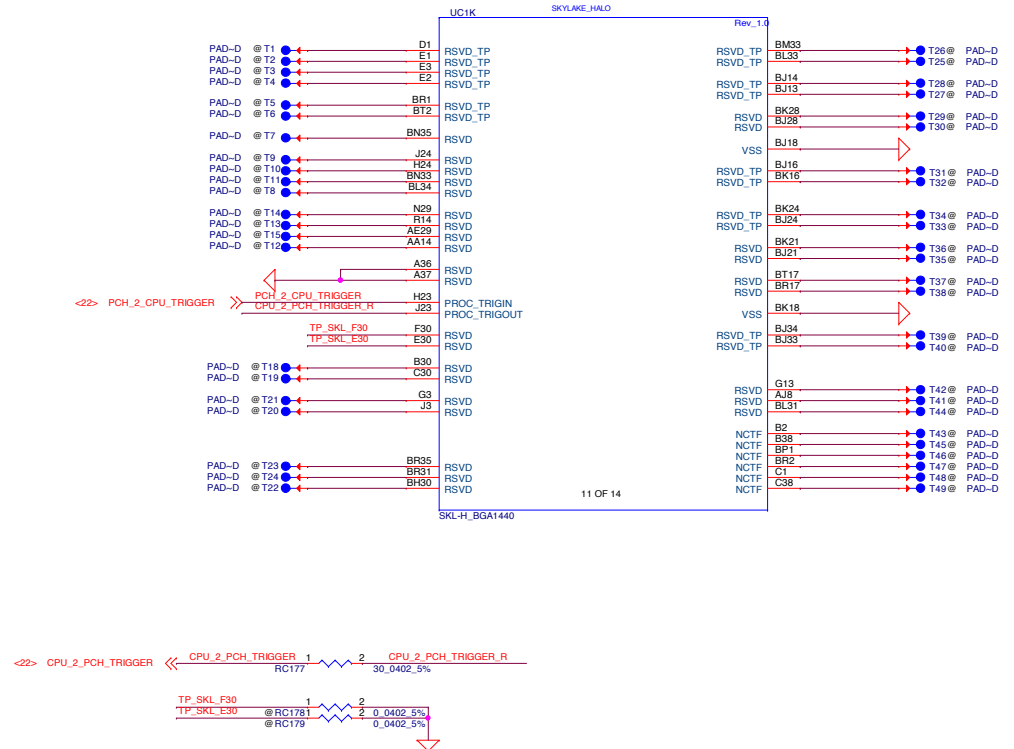
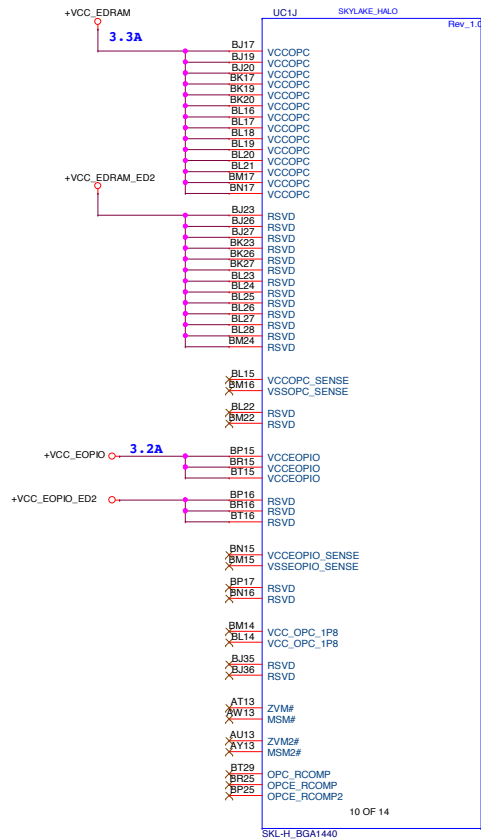






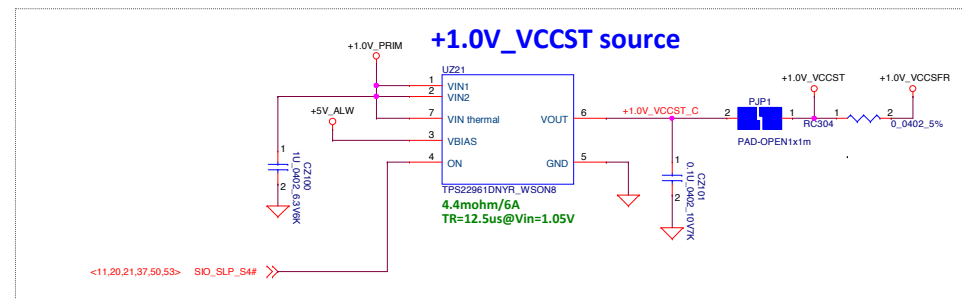
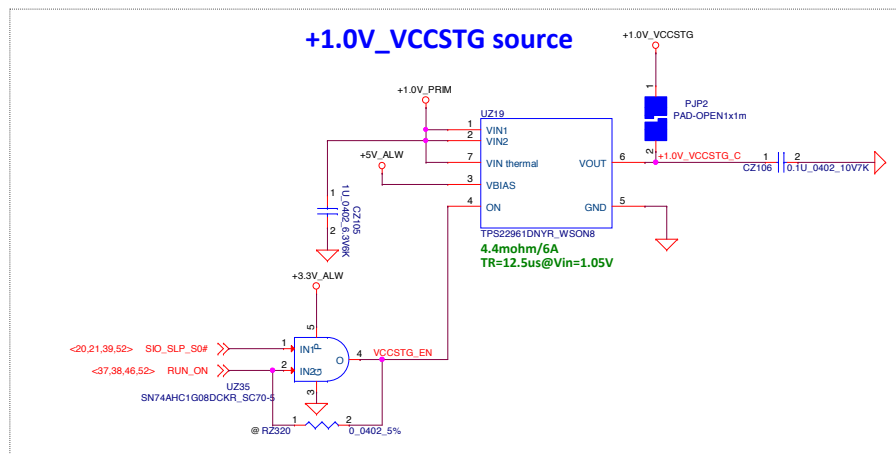
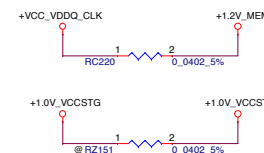
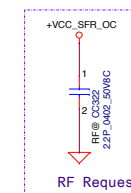
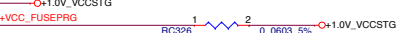
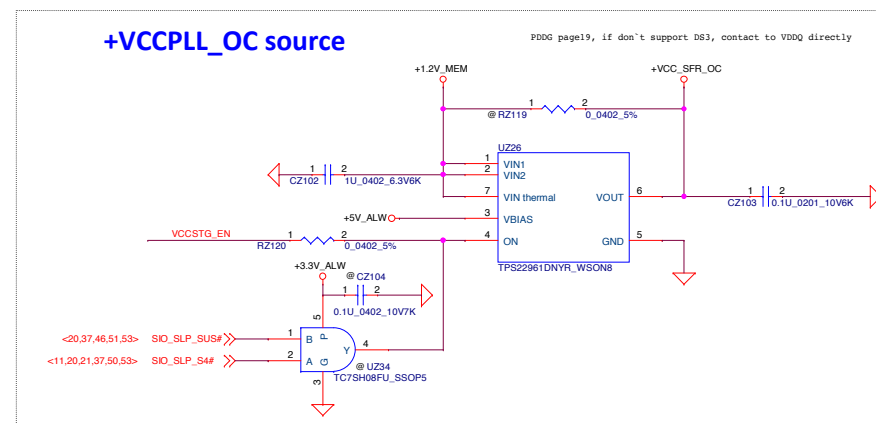
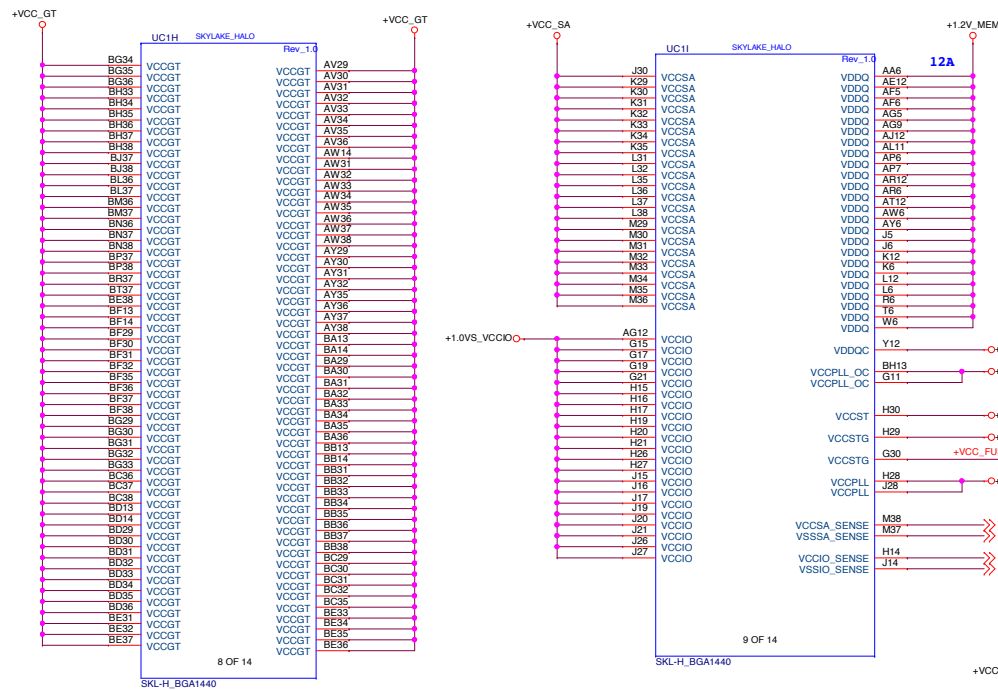


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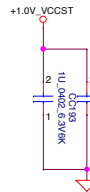
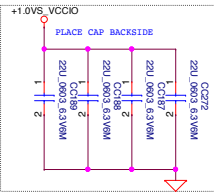
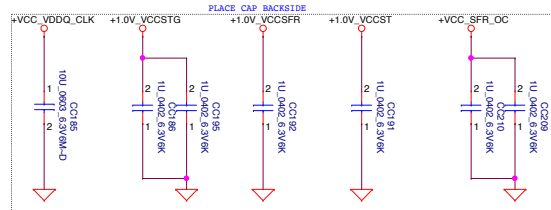
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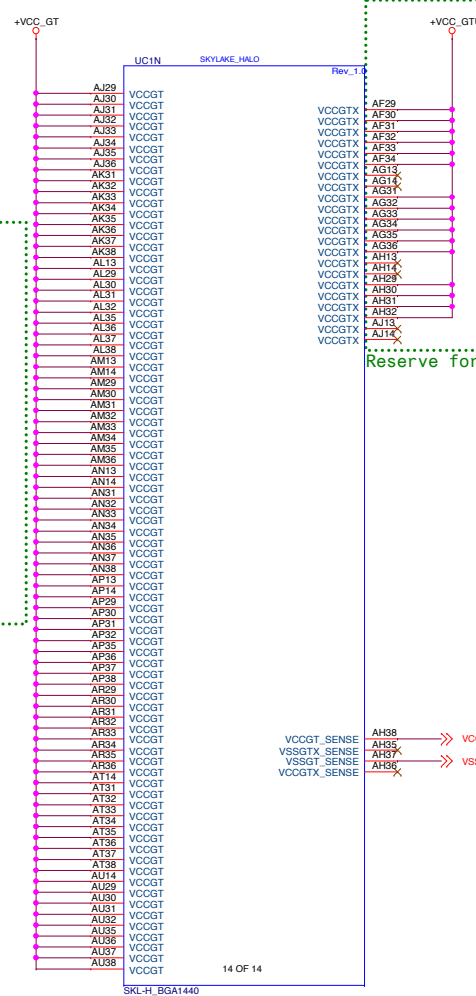
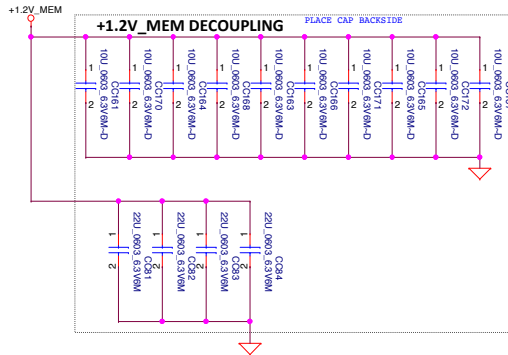


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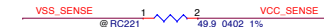
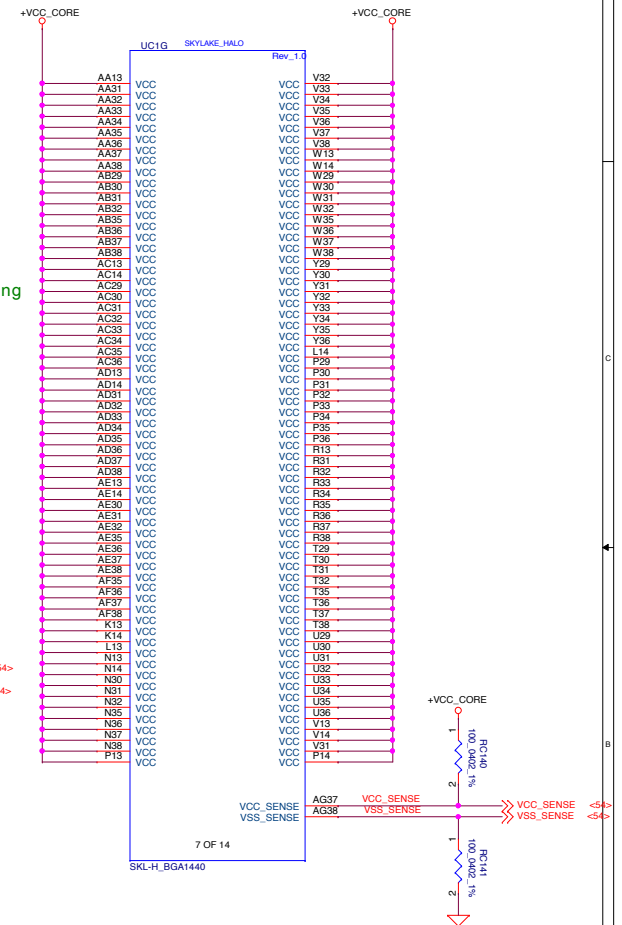
For SKL-H 4+2  
Remove VCCOPC/VCCEPIO/  
VCCOPC\_1P8 Cap



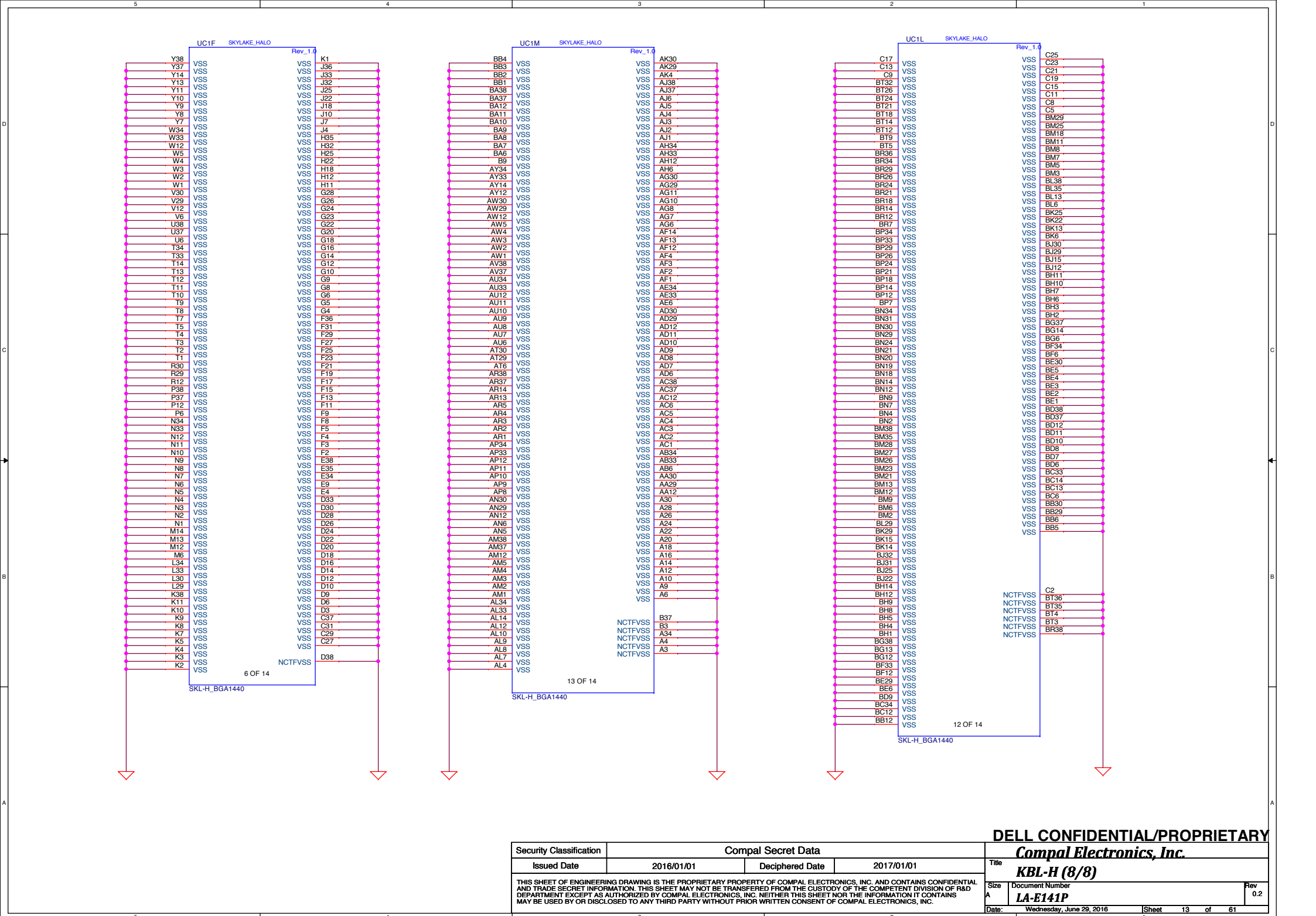
Remove to Power (+VCC\_SA cap)



Reserve for Soldering

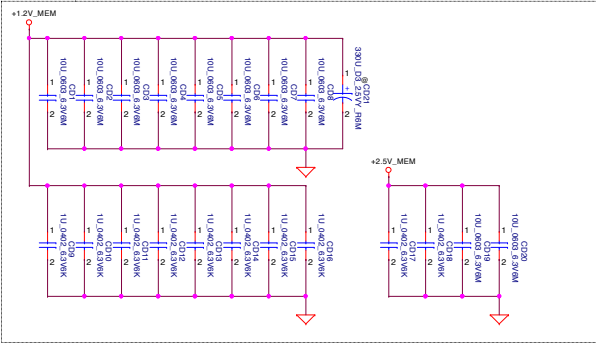


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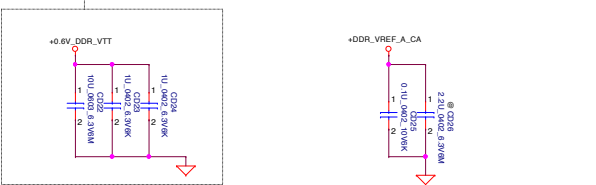


<B> DDR\_A\_DQS[0:7]  
 <B> DDR\_A\_DQ[0:7]  
 <B> DDR\_A\_DQ[15:31]  
 <B> DDR\_A\_DQ[32:47]  
 <B> DDR\_A\_DQ[48:63]  
 <B> DDR\_A\_MA[0:16]

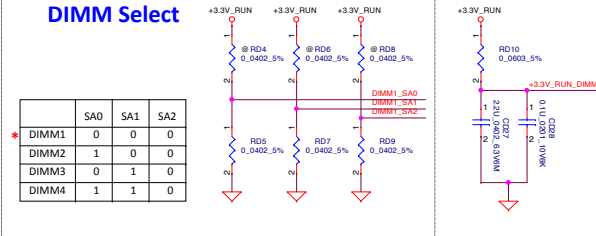
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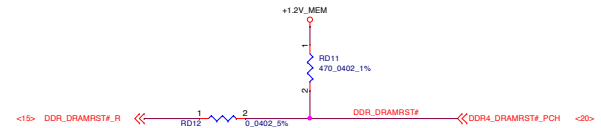
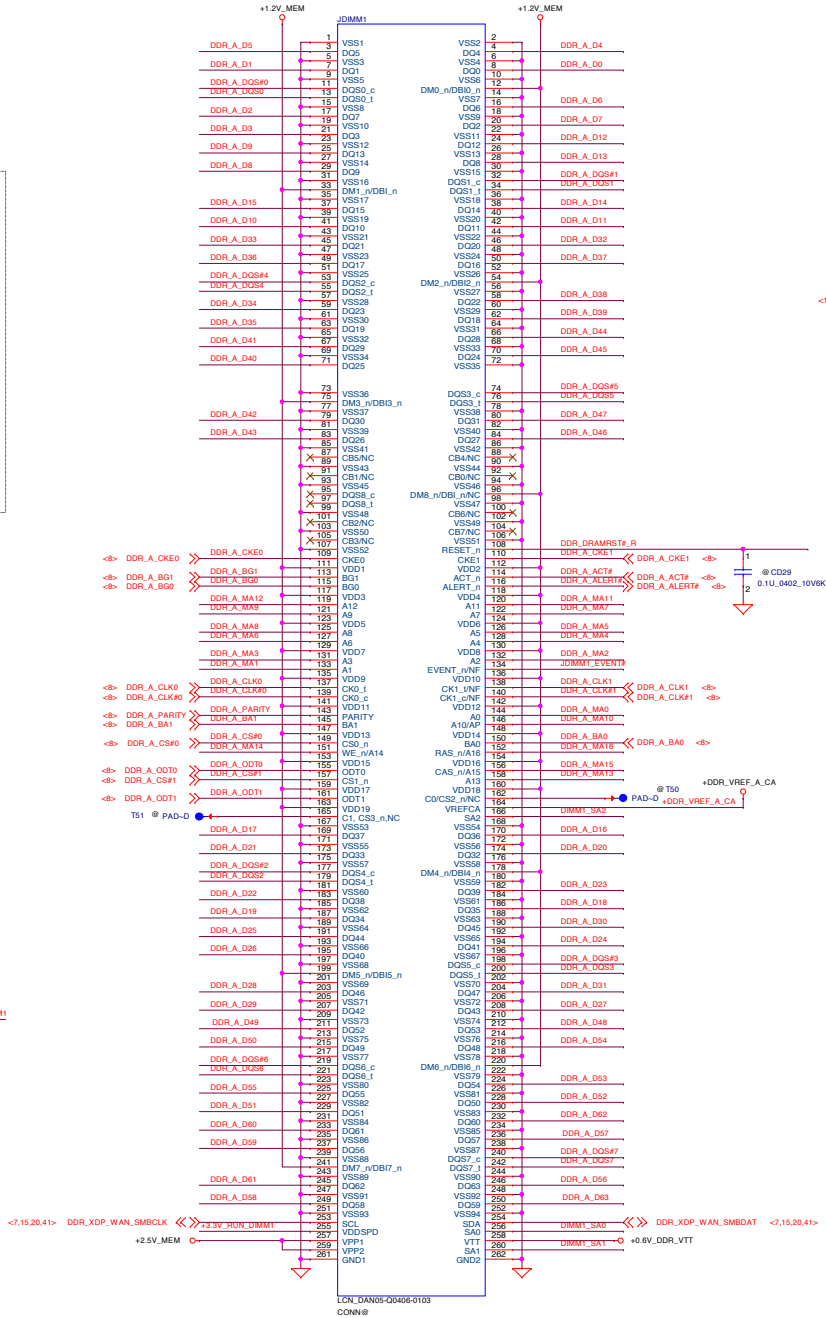
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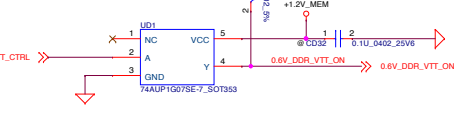
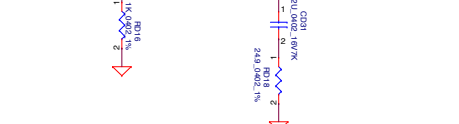
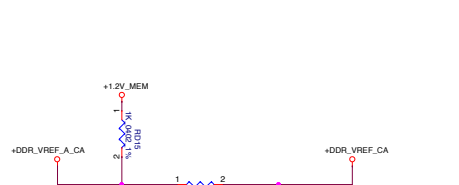
## DIMM Select



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Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]



<B> DDR\_A\_DQS[0:7]  
 <B> DDR\_A\_DQ[0:7]  
 <B> DDR\_A\_DQ[15:31]  
 <B> DDR\_A\_DQ[32:47]  
 <B> DDR\_A\_DQ[48:63]  
 <B> DDR\_A\_MA[0:16]



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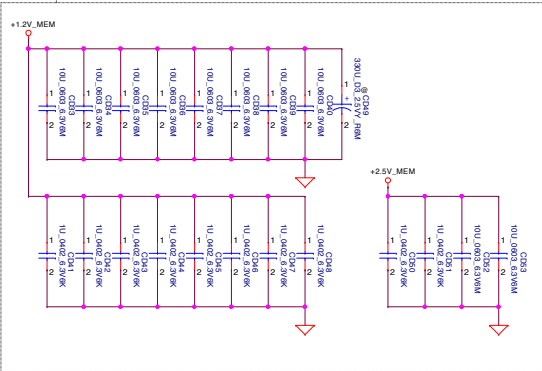
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DDR4-SODIMM SLOT1

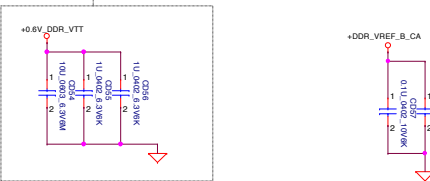
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DDR\_B\_DQS#0..7  
DDR\_B\_DQS#0..7  
DDR\_B\_DQ15..31  
DDR\_B\_DQ15..31  
DDR\_B\_DQ32..47  
DDR\_B\_DQ32..47  
DDR\_B\_DQ48..63  
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DDR\_B\_MA0..16

Layout Note:  
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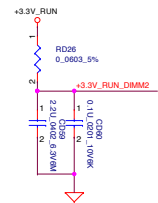
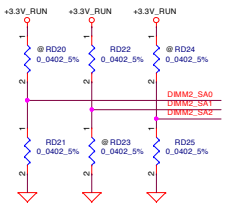


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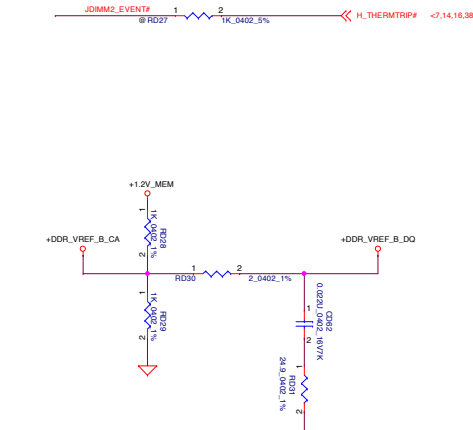


## DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



Byte[0]	DQ[7:0]	DQS/DQS#0]
Byte[1]	DQ[15:8]	DQS/DQS#1]
Byte[2]	DQ[23:16]	DQS/DQS#2]
Byte[3]	DQ[31:24]	DQS/DQS#3]
Byte[4]	DQ[39:32]	DQS/DQS#4]
Byte[5]	DQ[47:40]	DQS/DQS#5]
Byte[6]	DQ[55:48]	DQS/DQS#6]
Byte[7]	DQ[63:56]	DQS/DQS#7]

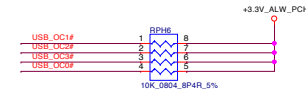
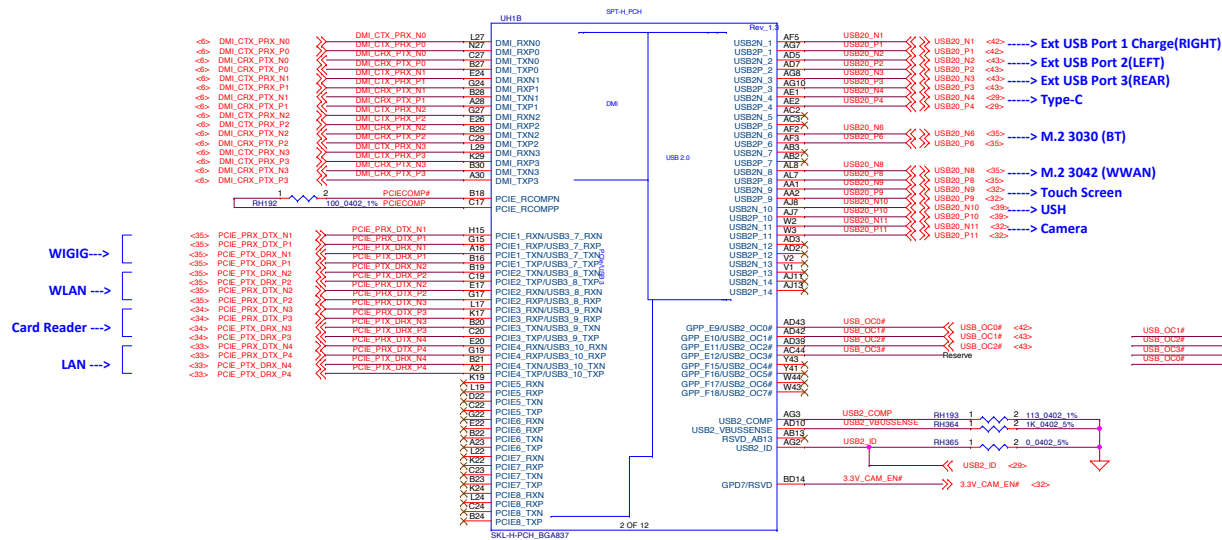
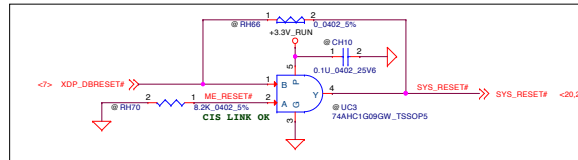


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DDR4-SODIMM SLOT2

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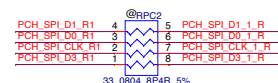
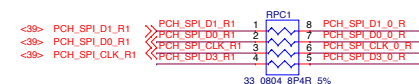
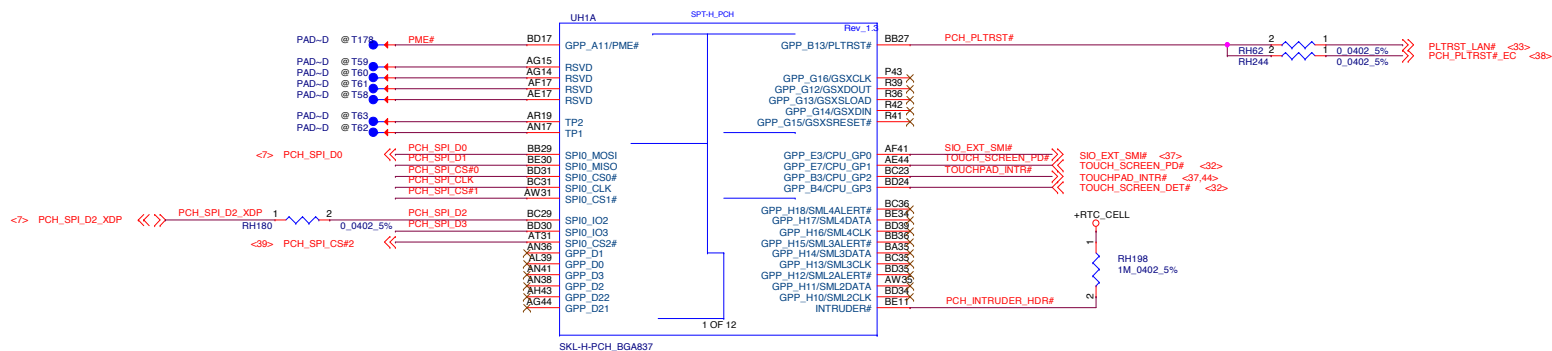
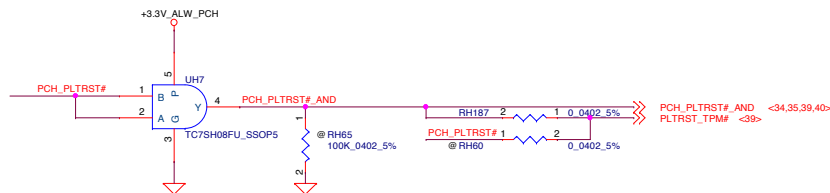
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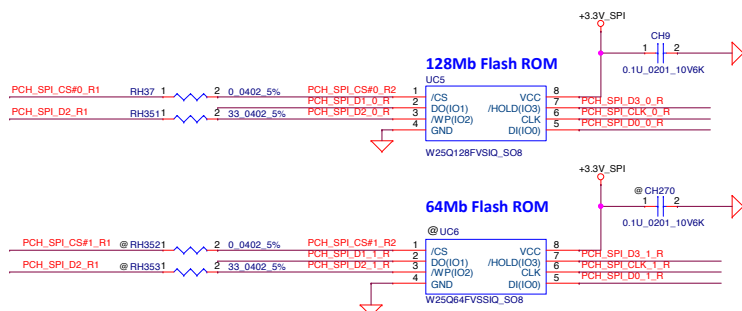
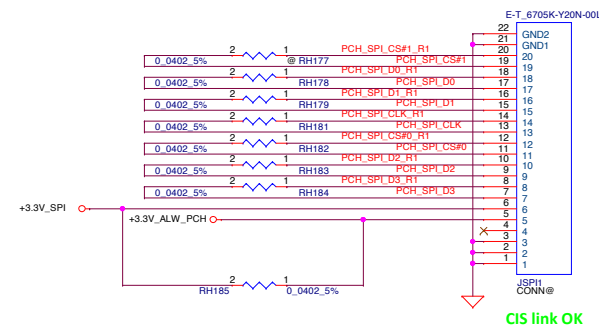
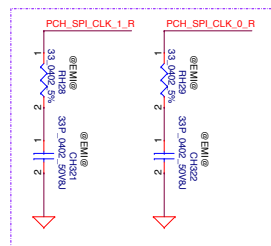
KABYLAKE PCH-H (2/9)

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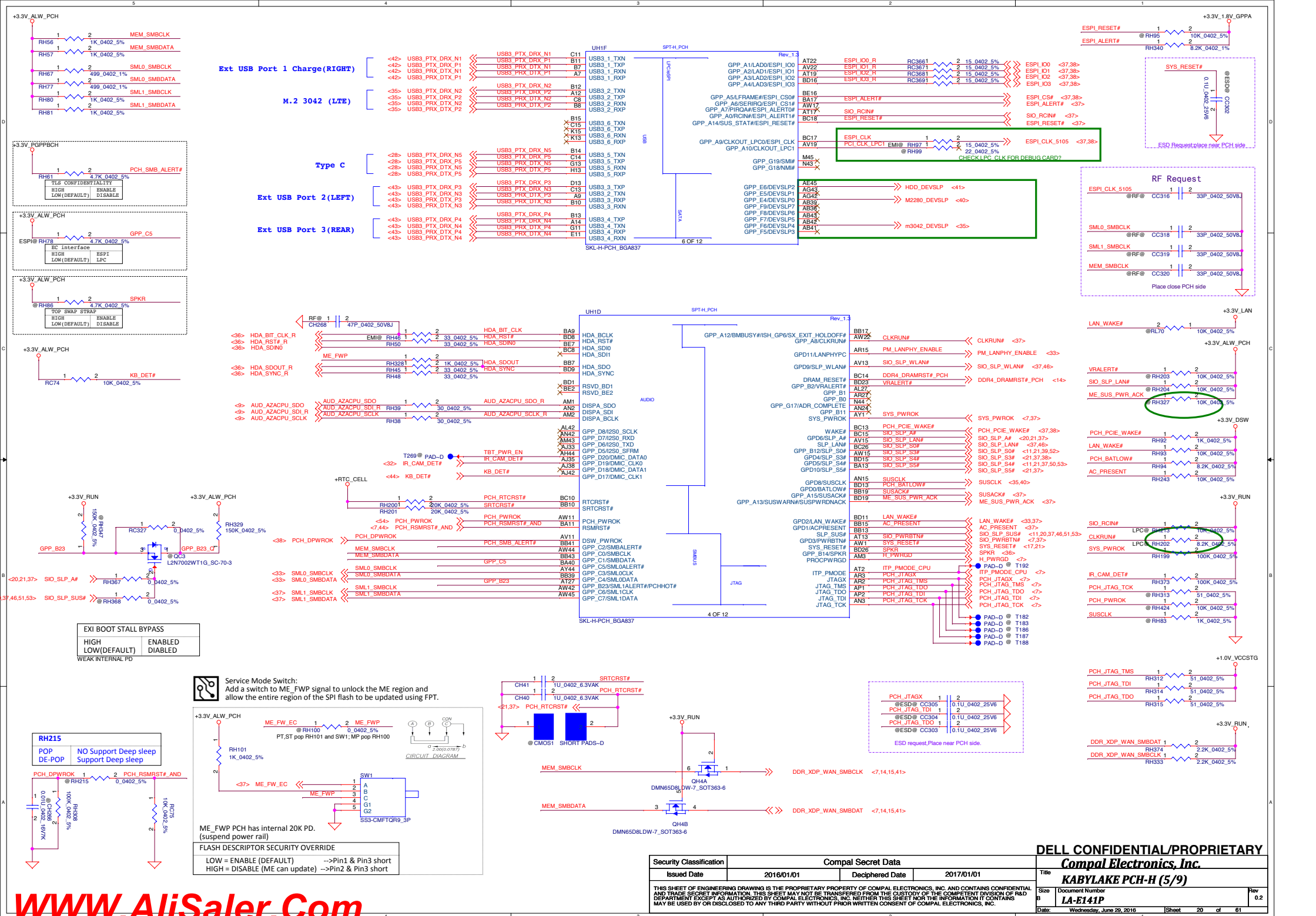


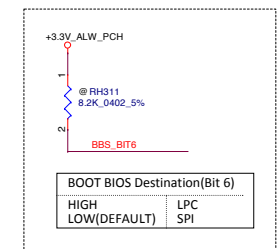
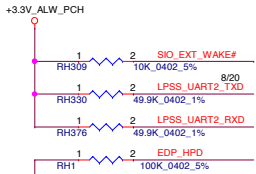
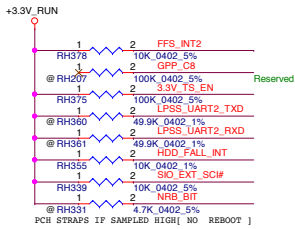
Note that the pull down resistor on SPI0\_IO3 is only needed for SKL U/Y platforms with FS and SKL S/H platforms with pre-FS1/FS1 samples.

Need check

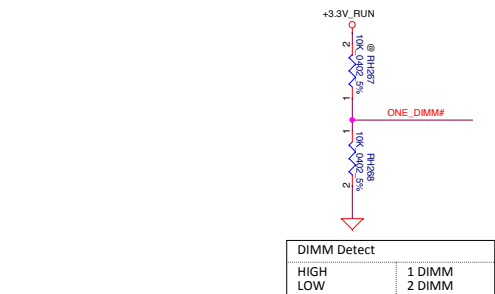
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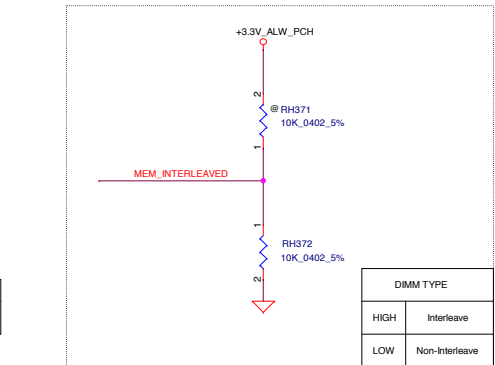
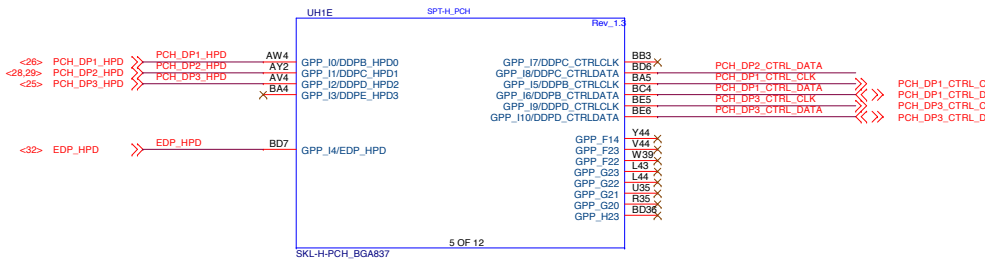
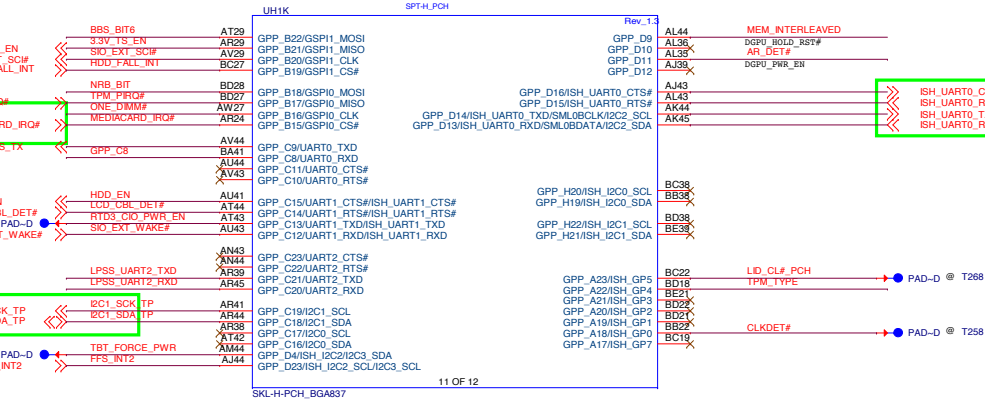




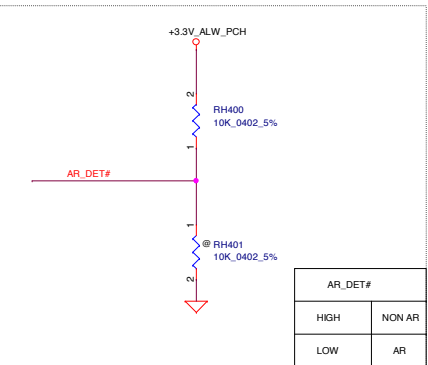
BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI



DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

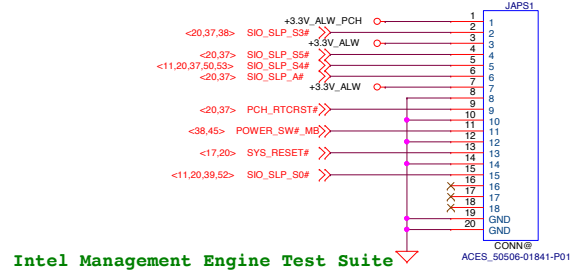


DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave



AR_DET#	
HIGH	NON AR
LOW	AR

Check ME about wire to board PN



Intel Management Engine Test Suite

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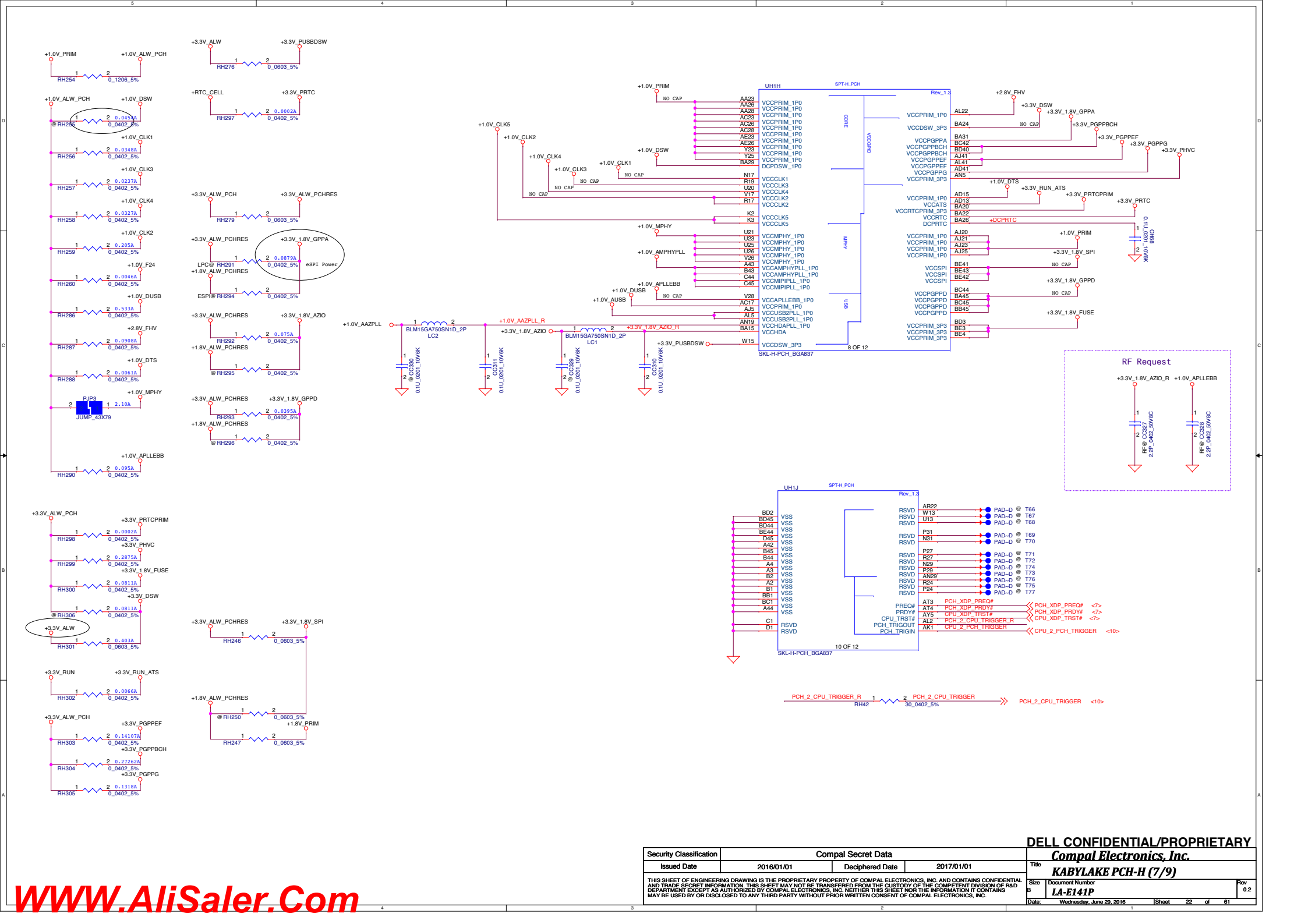
Compal Electronics, Inc.

KABYLAKE PCH-H (6/9)

LA-E141P

Wednesday, June 29, 2016

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UH11 SPT-H\_PCH Rev. 1.3

AC18	VSS	AR5
AN4	VSS	AR7
AN10	VSS	U15
BE14	VSS	AL4
BE18	VSS	AE29
BE23	VSS	AE4
BE28	VSS	AE42
BE32	VSS	AF18
BE37	VSS	AF20
BE40	VSS	AF21
BE9	VSS	AF23
C10	VSS	AF25
C2	VSS	AF26
C28	VSS	AF28
C37	VSS	AF29
J7	VSS	AG11
K10	VSS	AG13
K27	VSS	AG31
K33	VSS	AG32
K36	VSS	AG33
K4	VSS	AG38
K42	VSS	AG4
K43	VSS	AH1
L12	VSS	AH17
L13	VSS	AH18
L15	VSS	AH20
L4	VSS	AH21
L41	VSS	AH23
L8	VSS	AH25
M35	VSS	AH26
M42	VSS	AH28
N10	VSS	AH29
N15	VSS	AH45
N19	VSS	AJ10
N22	VSS	AJ14
N24	VSS	AJ15
N35	VSS	AJ17
N36	VSS	AJ18
N4	VSS	AJ26
N41	VSS	AJ28
N5	VSS	AJ29
P17	VSS	AJ31
P19	VSS	AJ32
P22	VSS	AJ36
P45	VSS	AK4
R10	VSS	AK42
R14	VSS	AL7
R22	VSS	AV17
R29	VSS	AV24
R33	VSS	AV27
R38	VSS	AV21
R5	VSS	AV33
T1	VSS	AV6
T2	VSS	AW13
T4	VSS	AW19
Y18	VSS	AW29
Y20	VSS	AW37
Y21	VSS	AW9
Y26	VSS	AY38
Y28	VSS	A145
Y29	VSS	B25
A18	VSS	B3
A25	VSS	B37
A32	VSS	B40
A37	VSS	B6
AA17	VSS	BAT
AA18	VSS	BB11
AA20	VSS	BB18
AA21	VSS	BB21
AA25	VSS	BB25
AA29	VSS	BB30
AA4	VSS	BB34
AA42	VSS	BC2
AB10	VSS	BD43
	VSS	

9 OF 12  
SKL-H-PCH\_BGA837

UH1L SPT-H\_PCH Rev. 1.3

C42	VSS	AB11
D10	VSS	AB7
D12	VSS	AB14
D15	VSS	AB31
D16	VSS	AB32
D17	VSS	AB38
D19	VSS	AB4
D21	VSS	AB5
D24	VSS	AC1
D25	VSS	AC20
D27	VSS	AC21
D29	VSS	AC25
D30	VSS	AC29
D31	VSS	AC45
D33	VSS	AB8
D35	VSS	AD11
D36	VSS	AD14
E13	VSS	AB15
E15	VSS	AD32
E31	VSS	AD33
E33	VSS	AD36
F44	VSS	AD4
F8	VSS	AD8
G42	VSS	AE18
G9	VSS	AE20
H17	VSS	AE21
H19	VSS	AE25
H22	VSS	AE28
H24	VSS	AL10
H27	VSS	AL11
H29	VSS	AL13
H3	VSS	AL17
H35	VSS	AL19
J10	VSS	AL24
J11	VSS	AL29
J3	VSS	AL32
J39	VSS	AL33
J5	VSS	AL38
J42	VSS	AM15
U10	VSS	AM17
U11	VSS	AM19
U14	VSS	AM22
U17	VSS	AM24
U18	VSS	AM27
U28	VSS	AM29
U29	VSS	AM45
U31	VSS	AN11
U32	VSS	AN22
U33	VSS	AN27
U38	VSS	AN31
U4	VSS	AN39
U8	VSS	AN7
V18	VSS	AN8
V20	VSS	AP11
V21	VSS	AP4
V23	VSS	AR33
V25	VSS	AR34
V29	VSS	AR42
V3	VSS	AR6
V45	VSS	AT10
W14	VSS	AT15
W31	VSS	AT36
W32	VSS	AT9
W33	VSS	AU1
W38	VSS	AU35
W4	VSS	AU36
W8	VSS	AU39
Y17	VSS	AU45
	VSS	C4

12 OF 12  
SKL-H-PCH\_BGA837

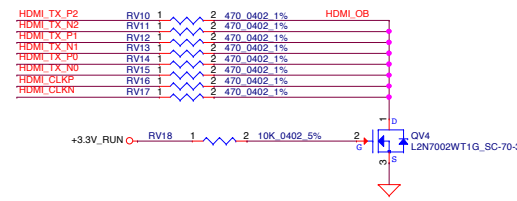
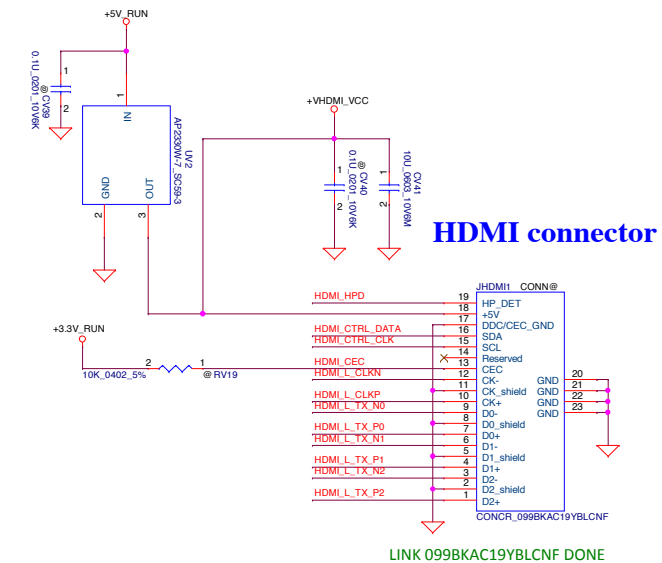
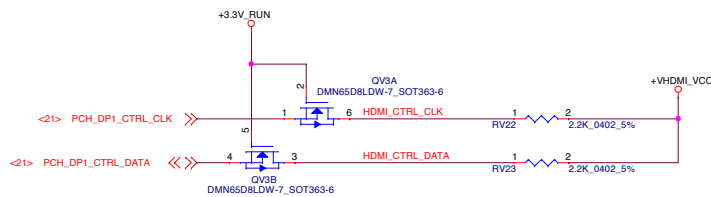
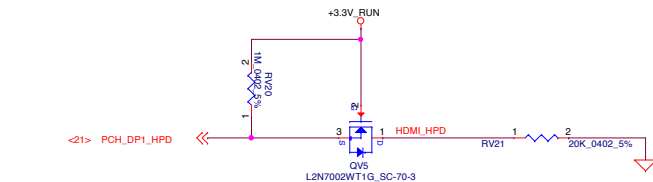
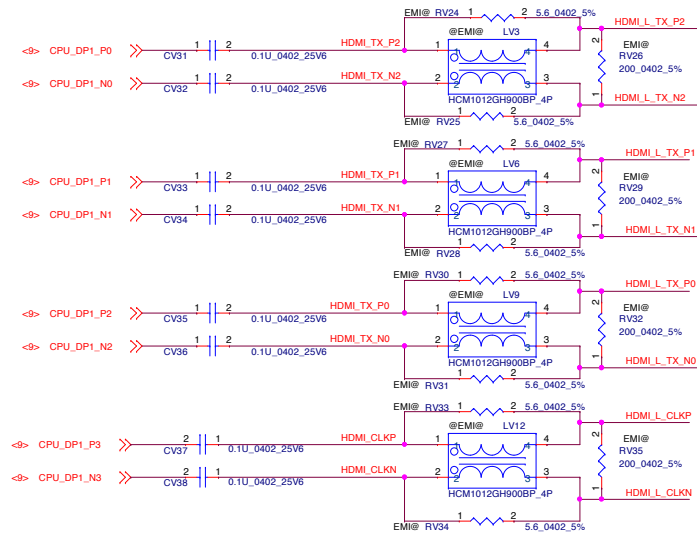
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Issued Date		Deciphered Date		Compal Electronics, Inc.	
2016/01/01		2017/01/01		Title	
				KABYLAKE PCH-H (9/9)	
				Size B	
				Document Number	
				LA-E141P	
				Date: Wednesday, June 29, 2016	
				Sheet 24 of 61	
				Rev 0.2	

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Size B	
Document Number	
LA-E141P	
Date: Wednesday, June 29, 2016	
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Rev 0.2	

Date: Wednesday, June 29, 2016		Sheet 25 of 61	
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# For Breckenridge 14



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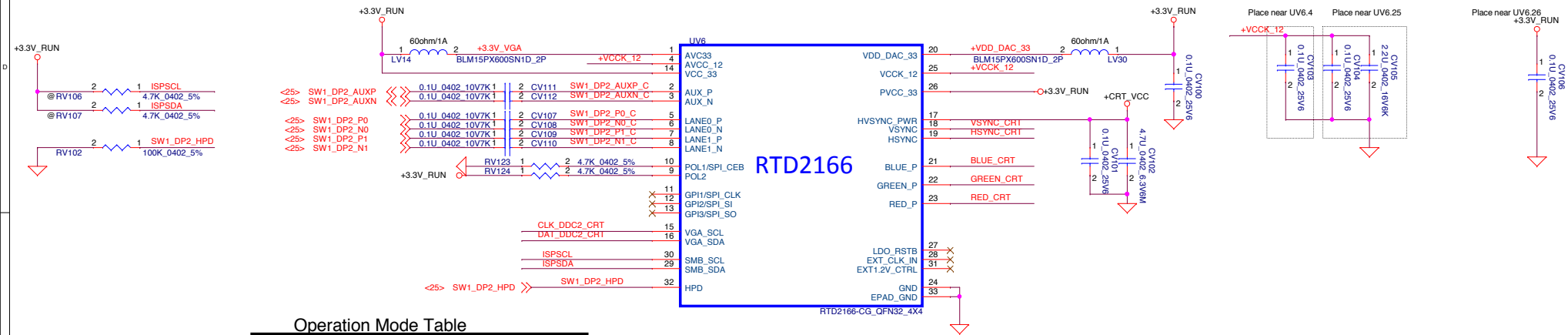
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Title	HDMI CONN		
Size	Document Number	Rev	0.2
Date	Wednesday, June 29, 2016	Sheet	26 of 61

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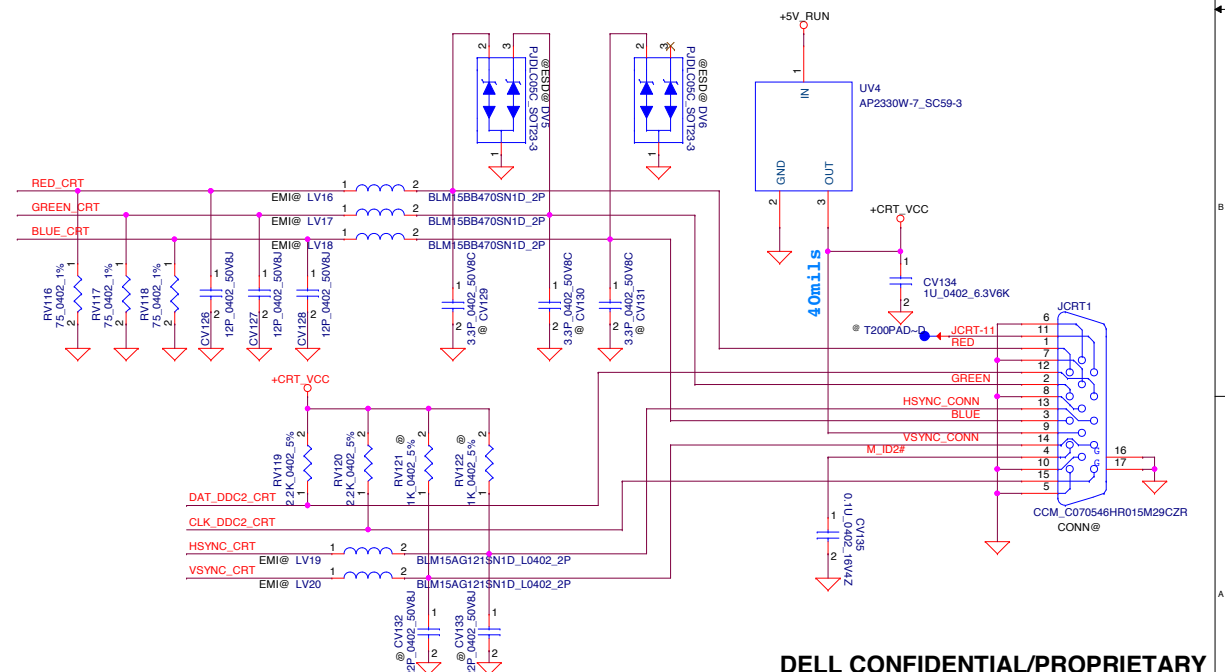
For TBT SW2\_DP2  
For non-TBT SW1\_DP2

## For Realtek Solution



### Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



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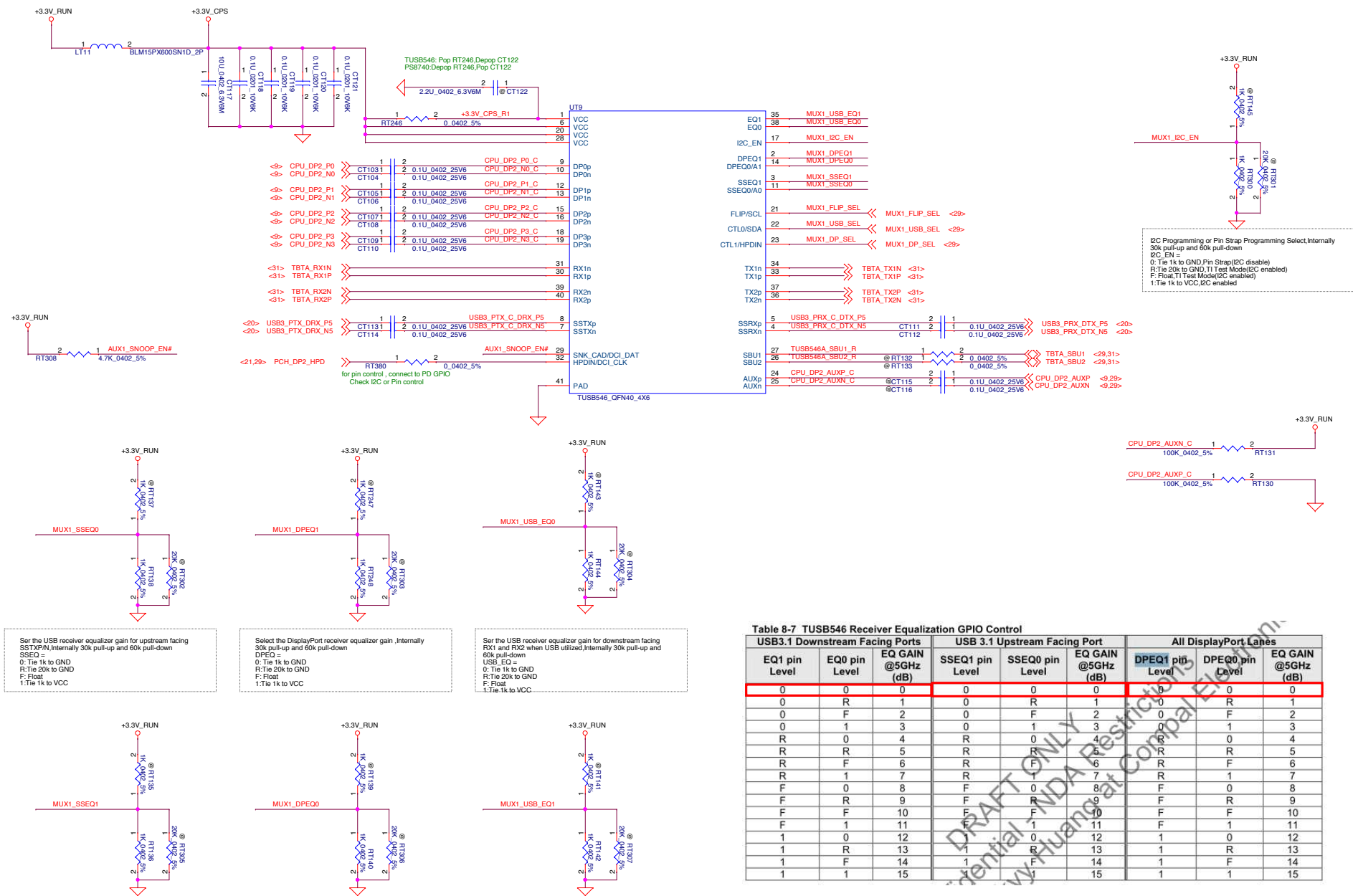
***Compal Electronics, Inc.***

### ***DP to VGA & VGA Conn***

Document Number  
**LA-E141P**

Rev  
0.2

Date: Wednesday, June 29, 2016		Sheet 27 of 61	
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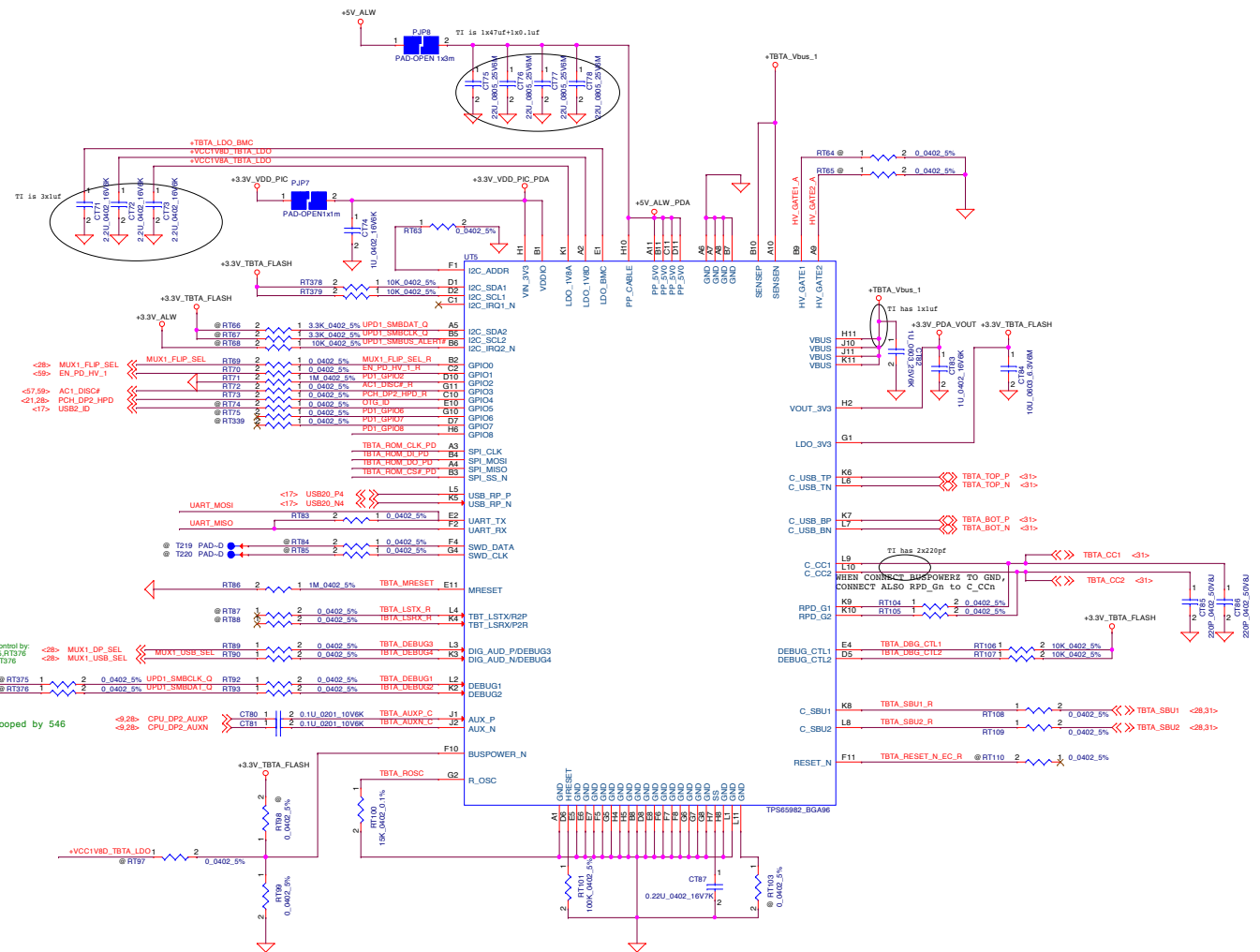
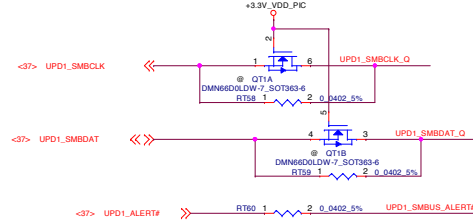
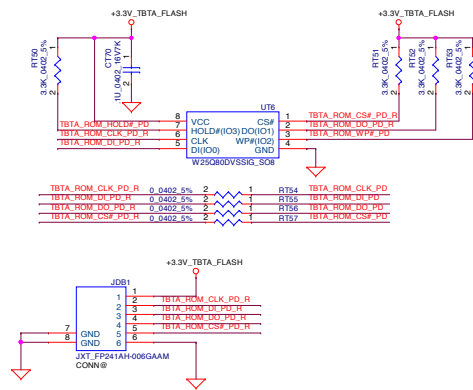
Set the USB receiver equalizer gain for upstream facing SSTXP/N, internally 30k pull-up and 60k pull-down  
 SSEQ =  
 0: Tie 1k to GND  
 R: Tie 20k to GND  
 F: Float  
 1: Tie 1k to VCC

Select the DisplayPort receiver equalizer gain, internally 30k pull-up and 60k pull-down  
 DPEQ =  
 0: Tie 1k to GND  
 R: Tie 20k to GND  
 F: Float  
 1: Tie 1k to VCC

Set the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB utilized, internally 30k pull-up and 60k pull-down  
 USB\_EQ =  
 0: Tie 1k to GND  
 R: Tie 20k to GND  
 F: Float  
 1: Tie 1k to VCC

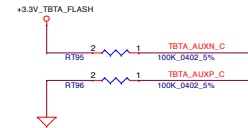
I2C Programming or Pin Strap Programming Select Internally  
 I2C\_EN =  
 0: Tie 1k to GND, Pin Strap (I2C disabled)  
 R: Tie 20k to GND, TI Test Mode (I2C enabled)  
 F: Float, TI Test Mode (I2C enabled)  
 1: Tie 1k to VCC, I2C enabled

For Non-AR config



DIV = R2 / (R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	<p>UFF only</p> <p>5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>T1 VID supported</p>
0.10	0.18	1	<p>UFF only</p> <p>5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes-Sink, C and D pin configuration</p> <p>T1 VID supported</p>
0.20	0.28	2	<p>UFF only</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>T1 VID supported</p>
0.30	0.38	3	<p>UFF only</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes-Sink, C and D pin configuration</p> <p>T1 VID supported</p>
0.40	0.48	4	<p>DRP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>T1 VID supported</p> <p>Accepts data and power role swaps, but does not initiate.</p>
0.50	0.58	5	<p>DRP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes- Source, C, D, and E pin configurations.</p> <p>T1 VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p>Accepts data role swap to DEP and can initiate.</p>
0.60	0.68	6	<p>DRP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes- Source, C, D, and E pin configurations.</p> <p>T1 VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p>Accepts data role swap to DEP and can initiate.</p>
0.70	1.00	7	Infinite boot retry from Flash to Host IF cycles.

Route in pass through manner so AUX can be snooped by 546

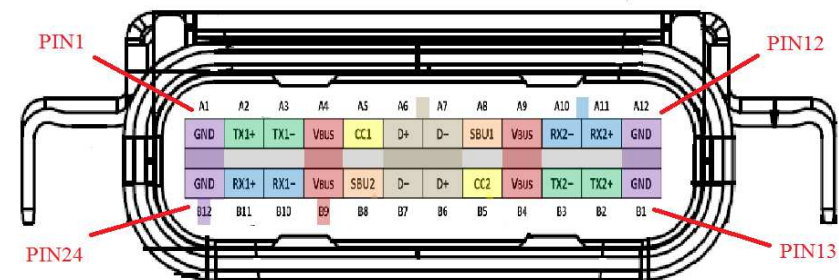
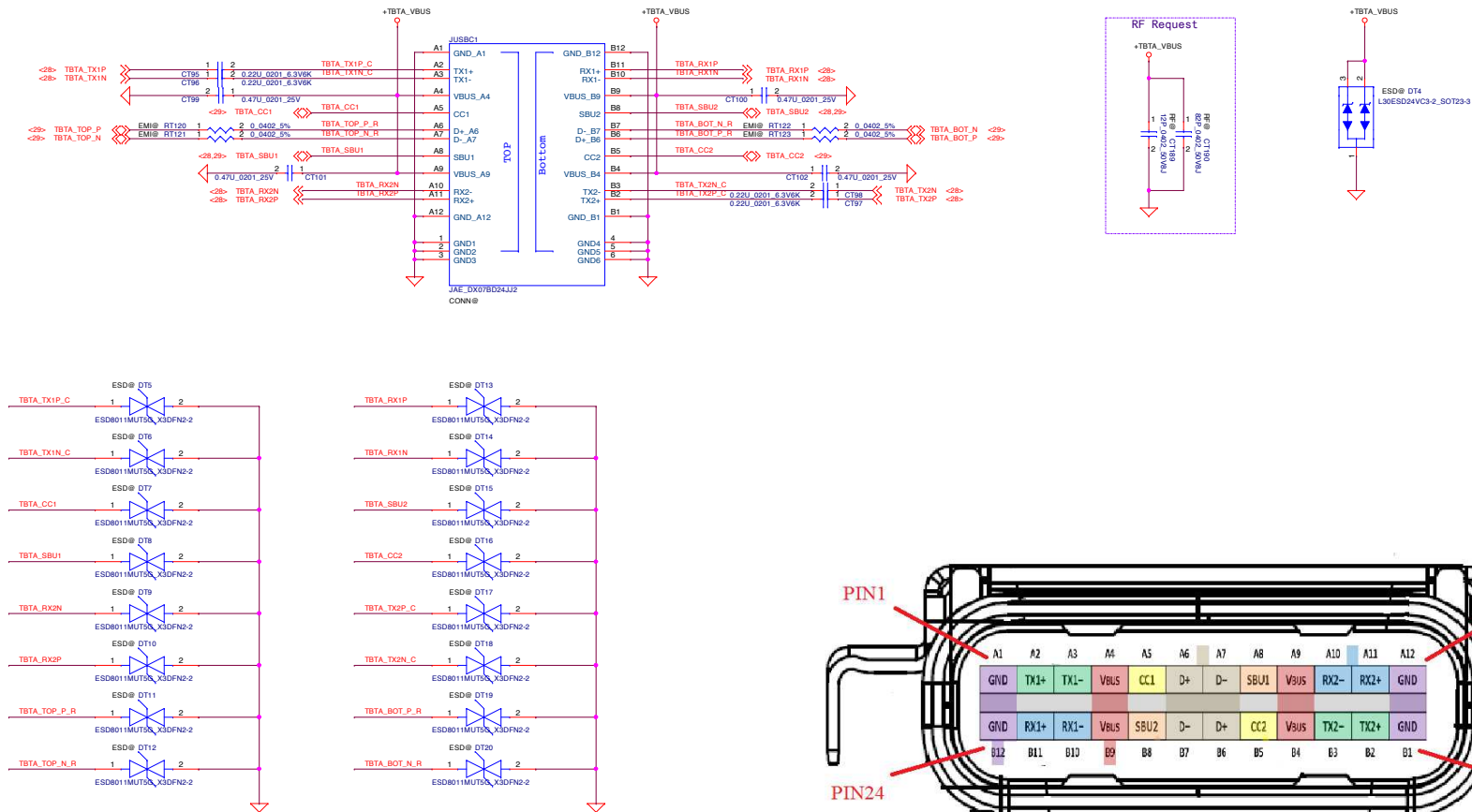


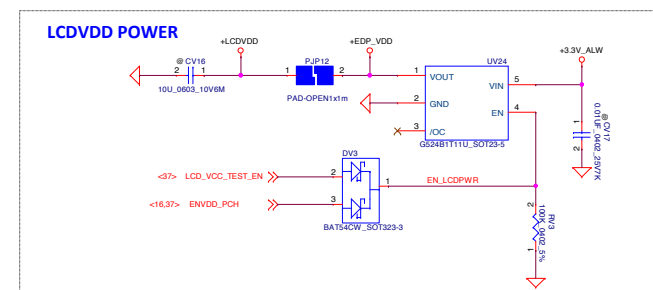
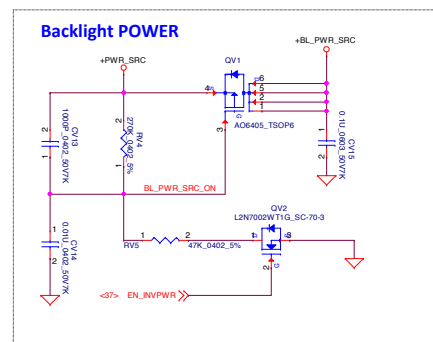
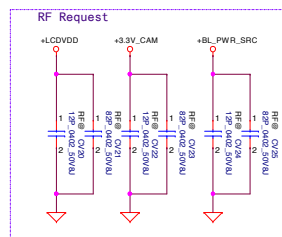
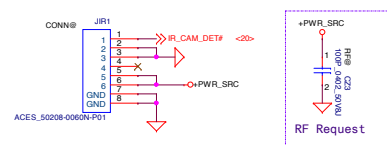
Need Link TPS65982D

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LA-VEP16-000001				Sheet	of
61				61	61



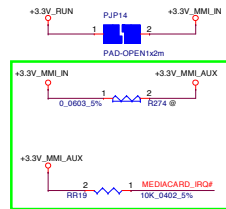






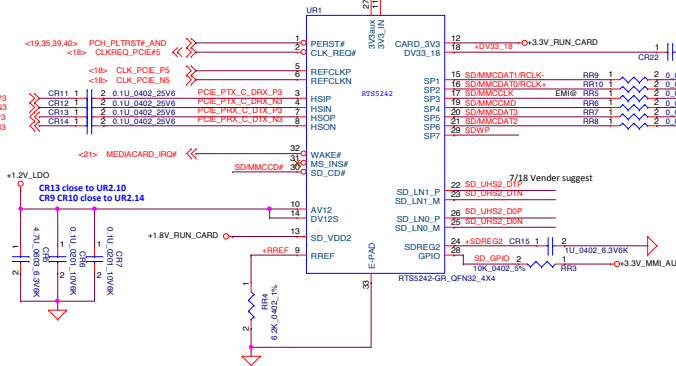
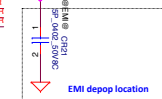
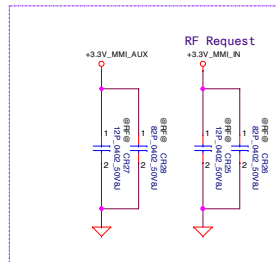
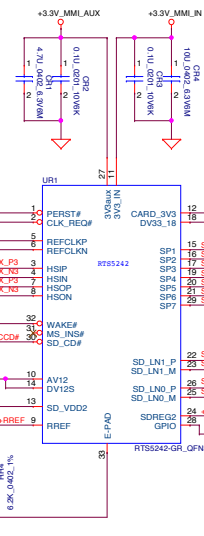


### For PCIe Interface

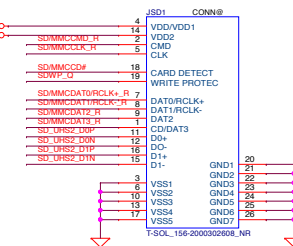
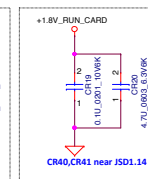
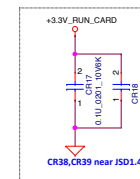
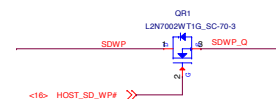


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.

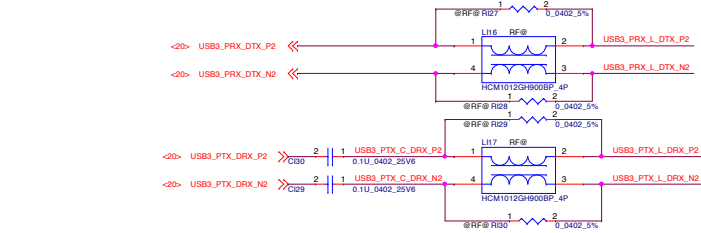
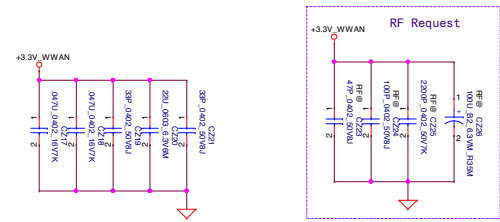
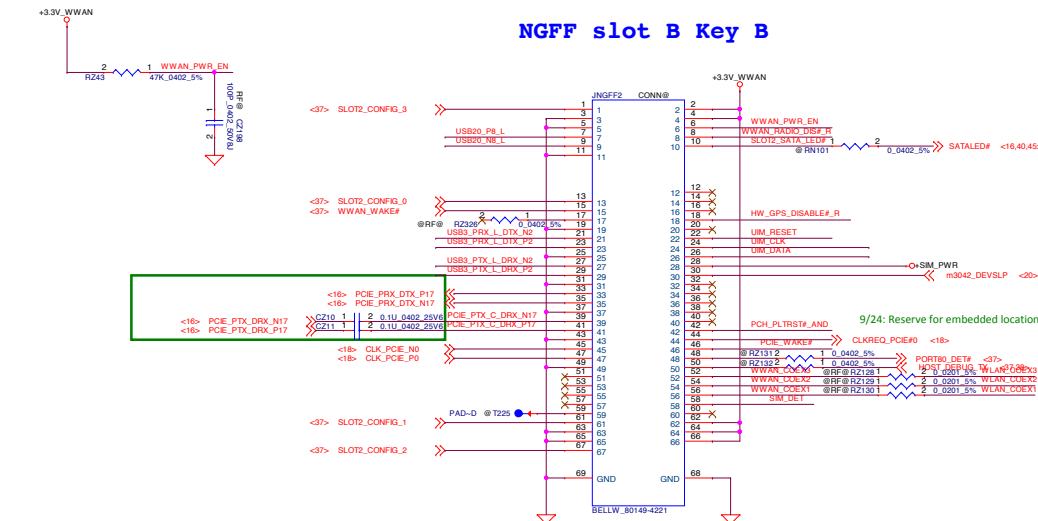


HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)

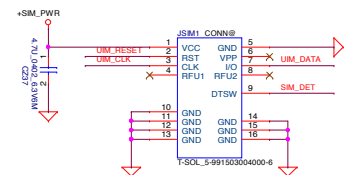


LINK SP070011U00 DONE

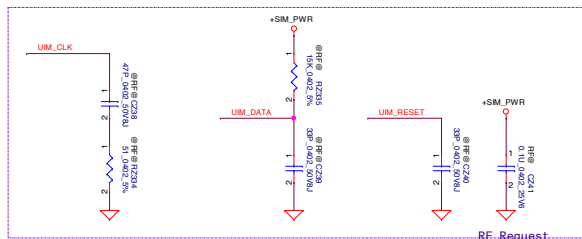
## NGFF slot B Key B



## SIM Card Push-Push



T-SOL\_5-991503004000-6 LINK DONE



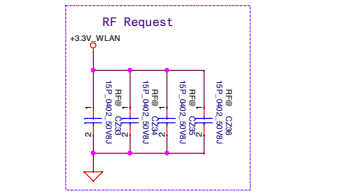
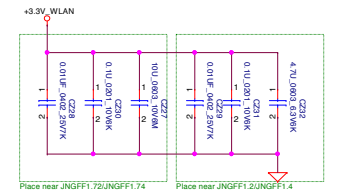
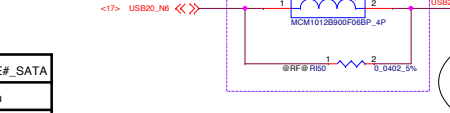
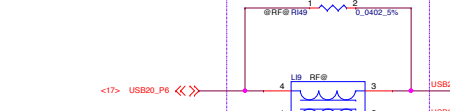
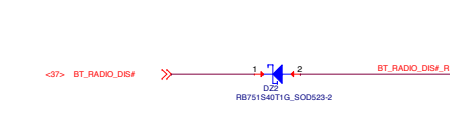
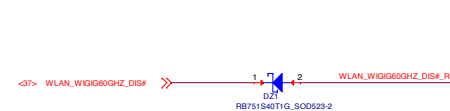
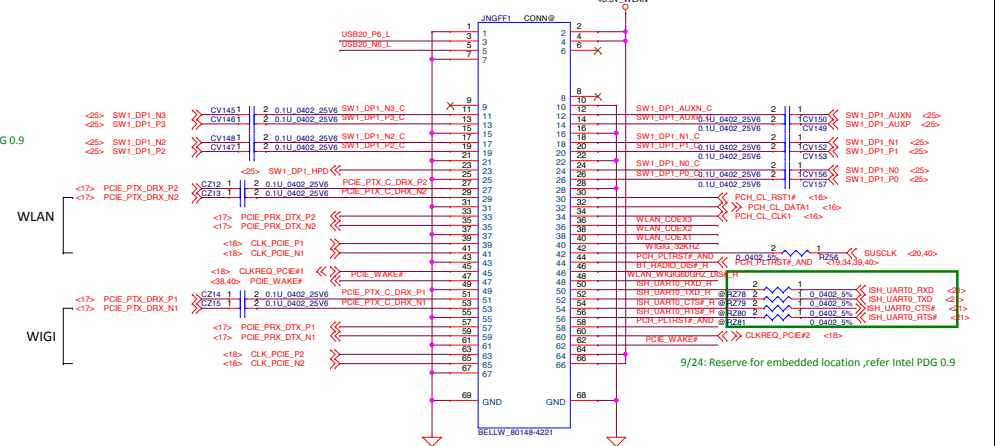
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	m3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIe(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIe(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

for Brekenridge 12/14/15 UMA

For TBT SW2\_DP1  
For non-TBT SW1\_DP1

## NGFF slot A Key A

80148-3221&80148-4221 Footprint the same



## Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power Peak	Aux Power Normal
+3.3V			

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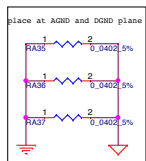
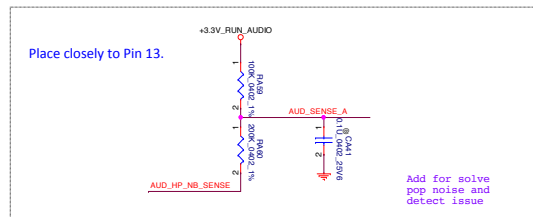
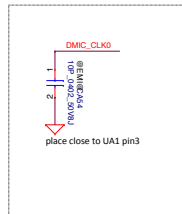
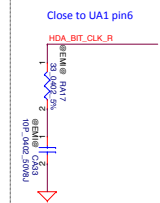
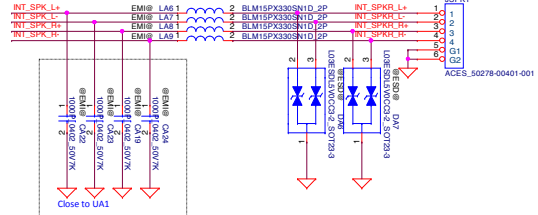
NGFF Card

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1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box)

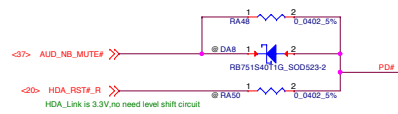
## Internal Speakers Header

40 mils trace keep 20 mil spacing

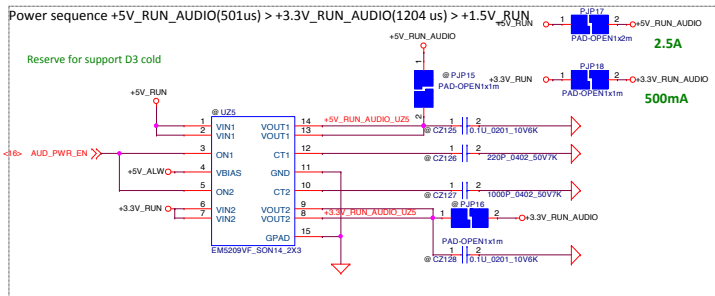


Add for solve pop noise and detect issue

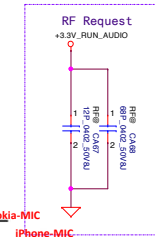
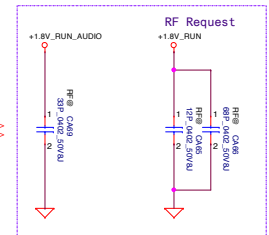
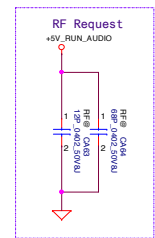
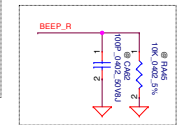
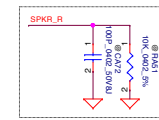
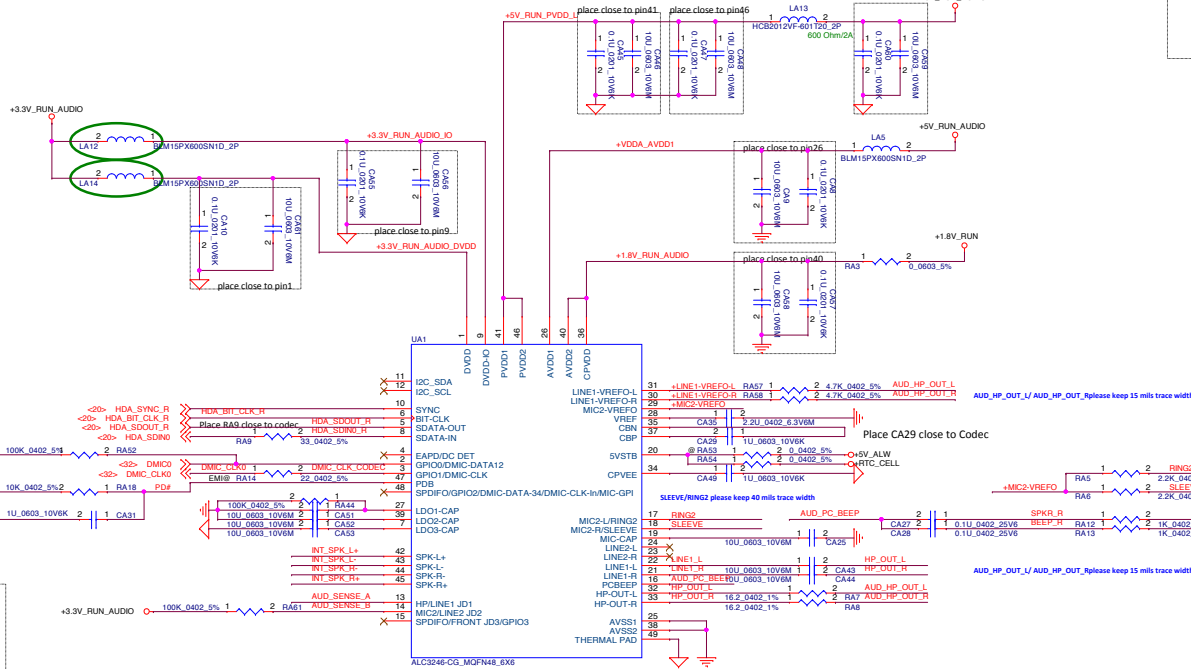
## CLASS-D POWER DOWN CONTROL CIRCUIT



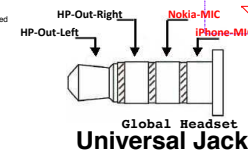
RES13 is one control line if DVDD is 3.3V (2x2 trace control lines)



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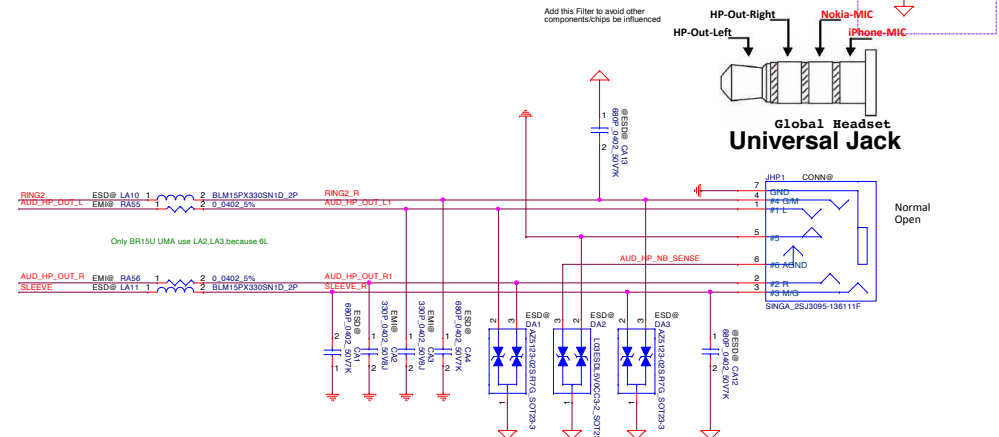


Add this Filter to avoid other components/chips be influenced



Global Headset

Normal Open



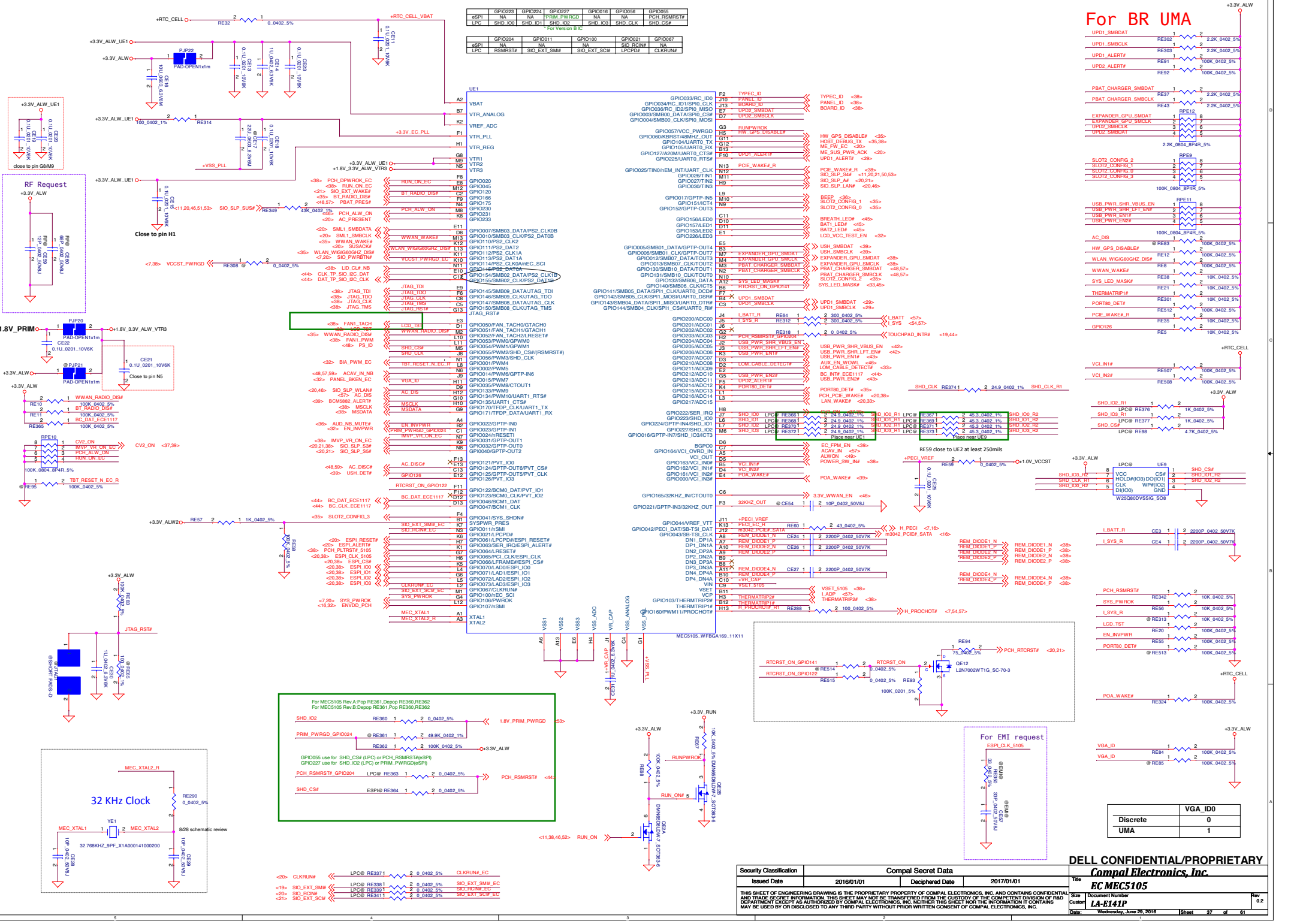
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Date:	Wednesday, June 29, 2016	Sheet	36	of 61

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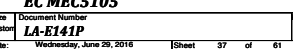
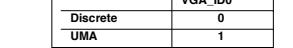
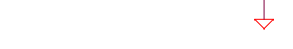
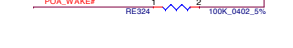
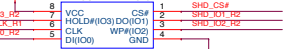
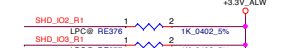
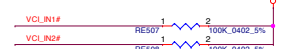
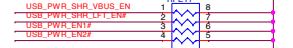
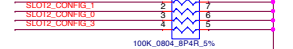
Compal Electronics, Inc.

Codec ALC3246





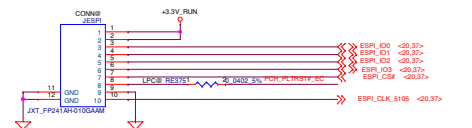
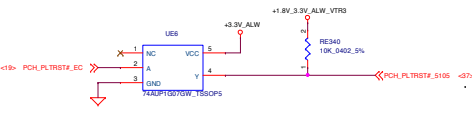
For BR UMA



Discrete	UMA
VGA_ID0	0
VGA_ID1	1

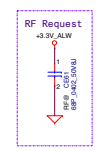
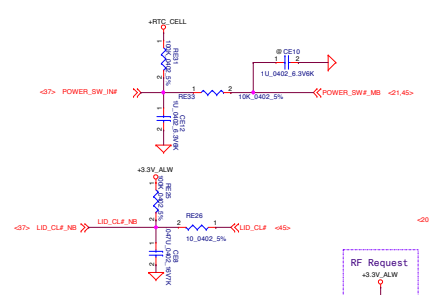
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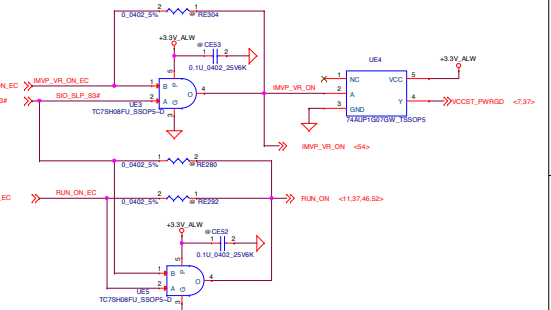
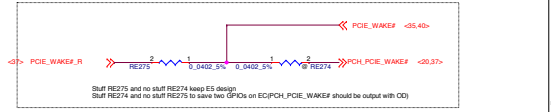


LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	



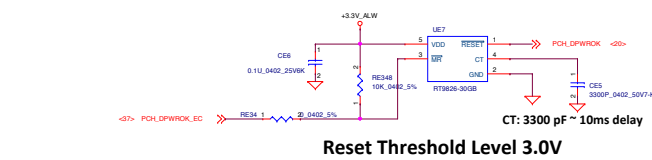
RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	



RE79	CE40	REV
240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	BR15 H
4.3K	4700p	BR15 P

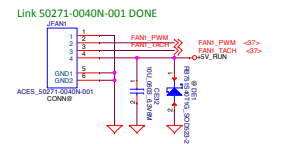
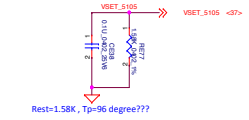
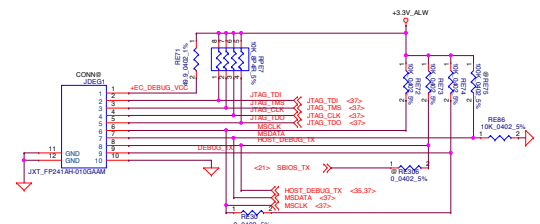
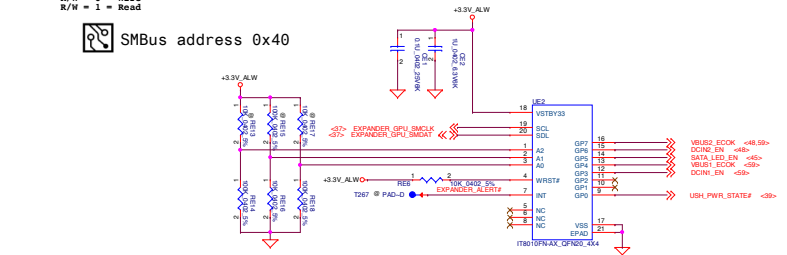
PD\_ACE\_DET# rise time is measured from 5%~68% BOARD\_ID rise time is measured from 5%~68% PANEL\_ID rise time is measured from 5%~68%



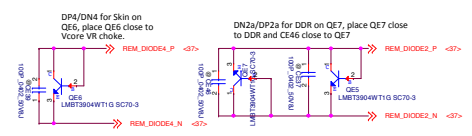
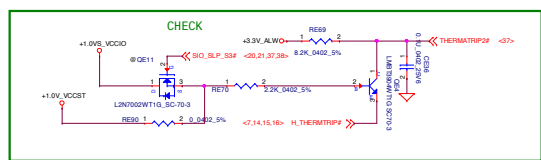
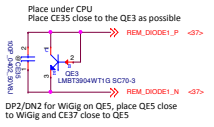
Reset Threshold Level 3.0V

Control Byte
0 1 0 0 A2 A1 A0 R/W
R/W = 0 = Write
R/W = 1 = Read

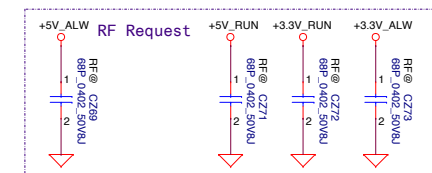
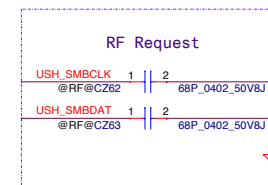
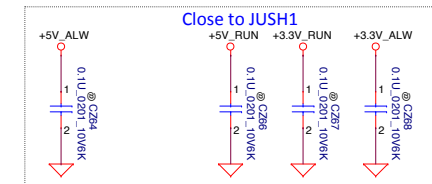
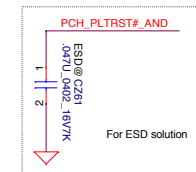
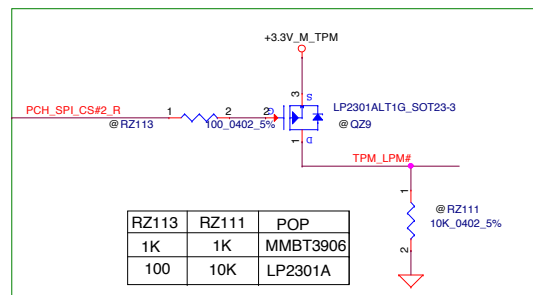
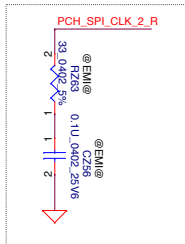
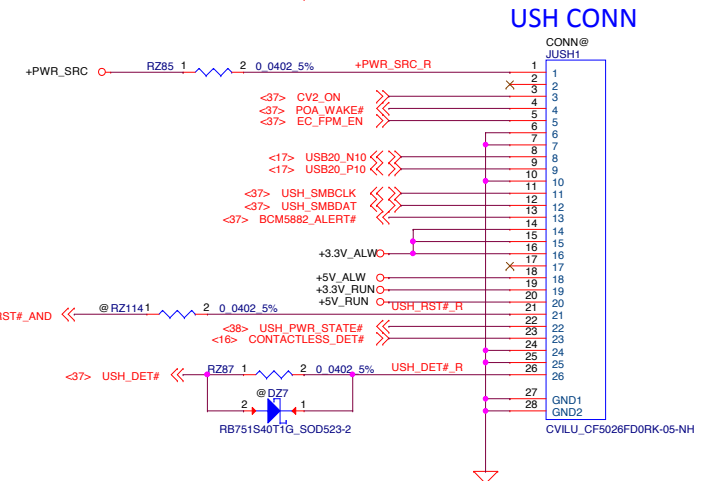
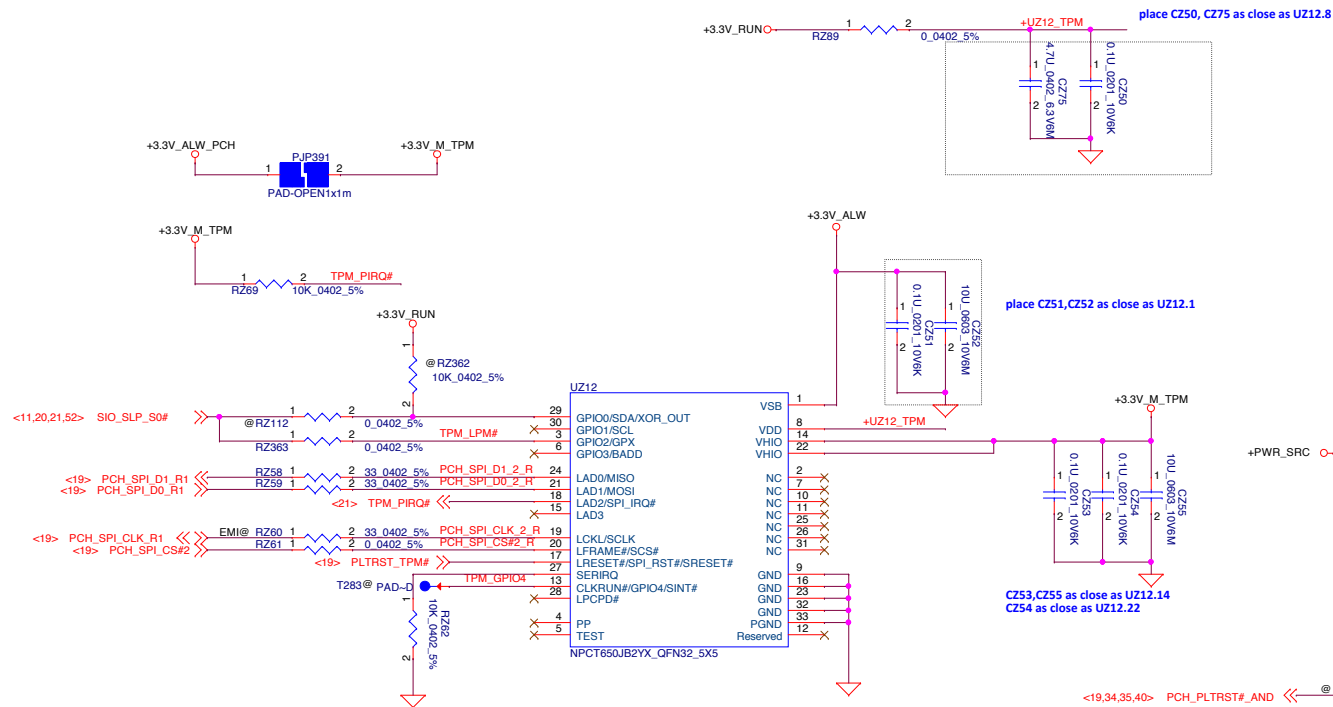
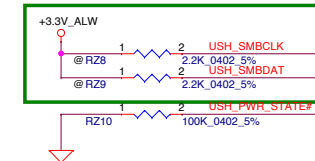
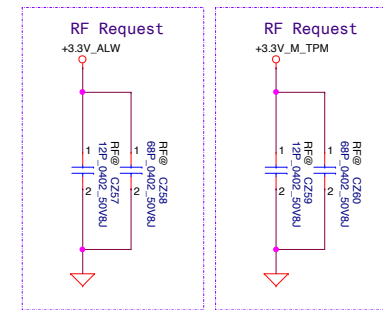
SMbus address 0x40



5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

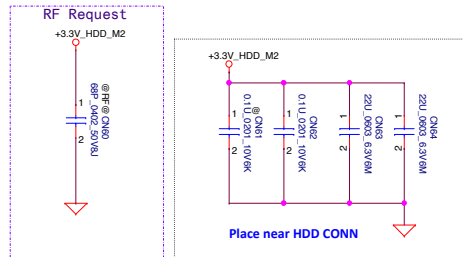


For NUVOTON TPM



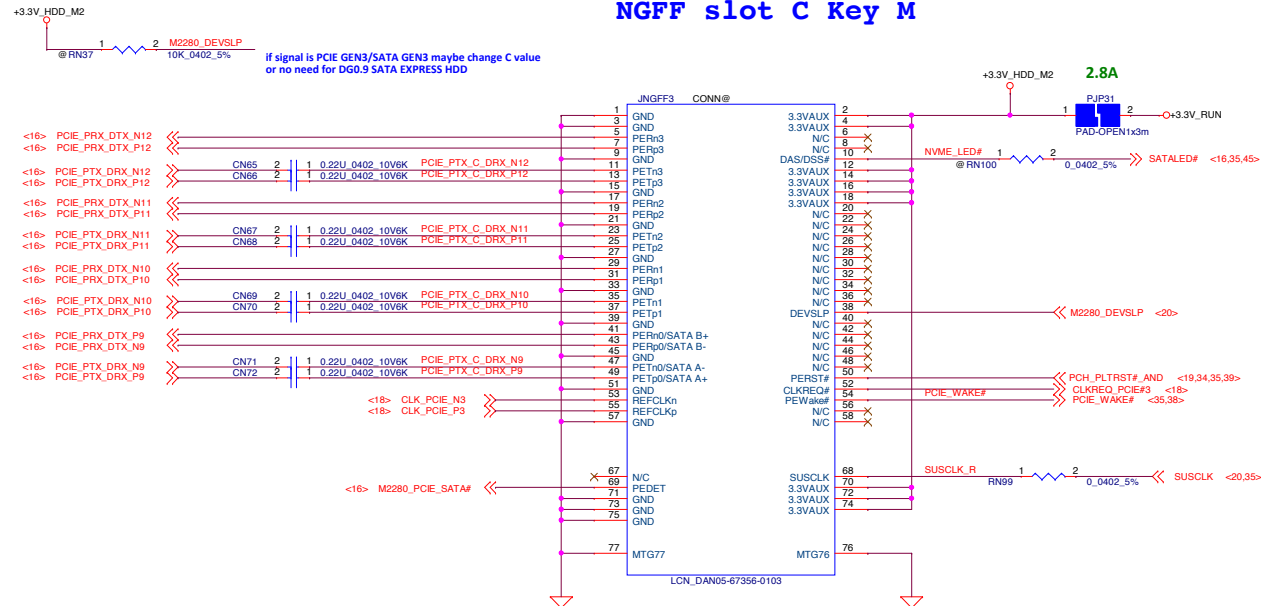
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For Breckenridge 15



2280 SSD

NGFF slot C Key M



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## **M2 2280 Socket**

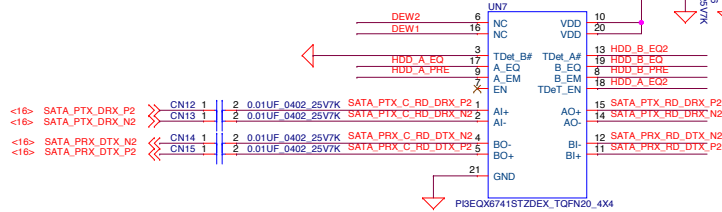
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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDeT_B#	NC	TDeT_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

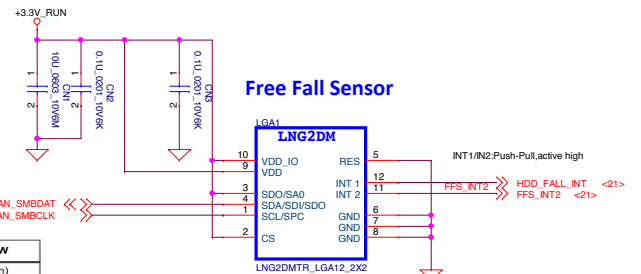
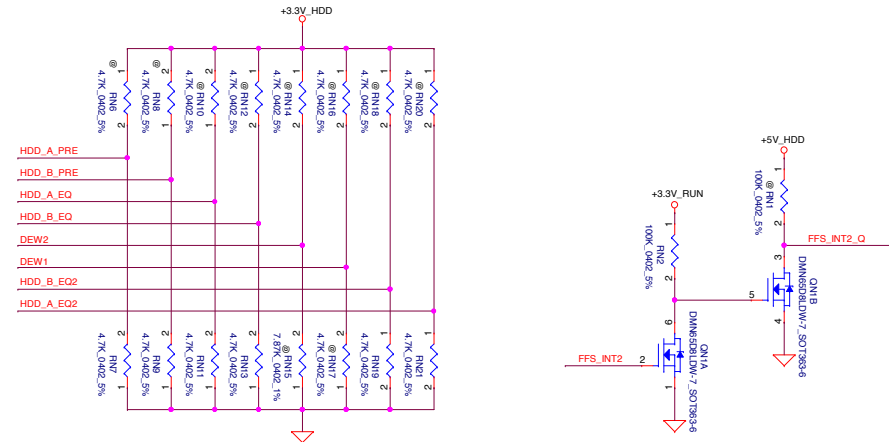
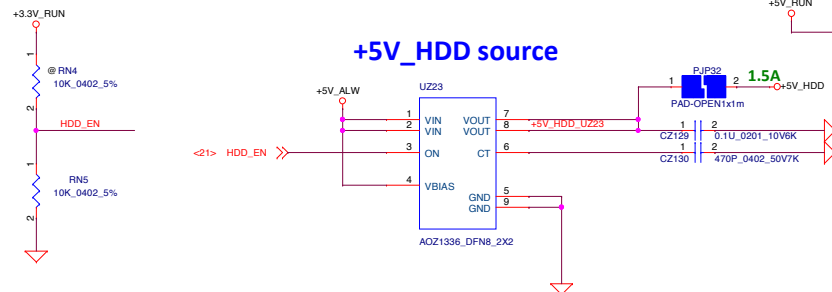
## SATA Repeater



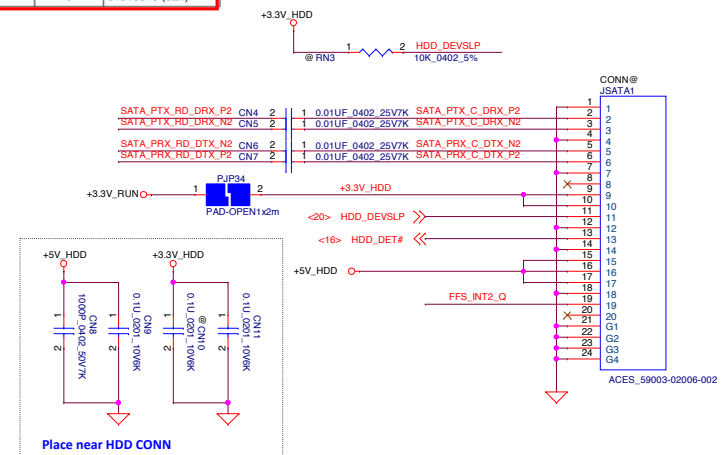
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	PD (RN5)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 9dB 14dB	7dB 9dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 NC 1	0dB -3.5dB -1.5dB	0dB -3.5dB -1.5dB

\* red color is current setting



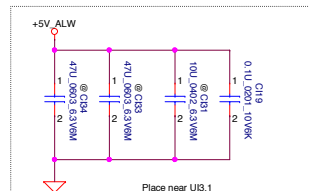
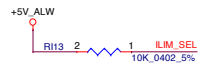
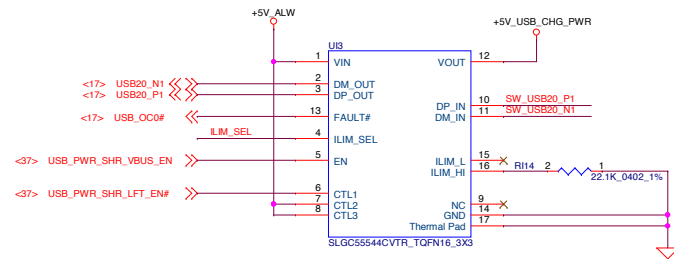
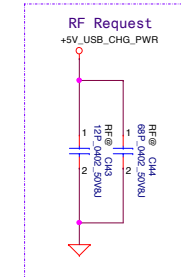
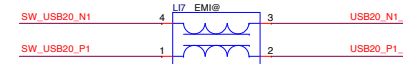
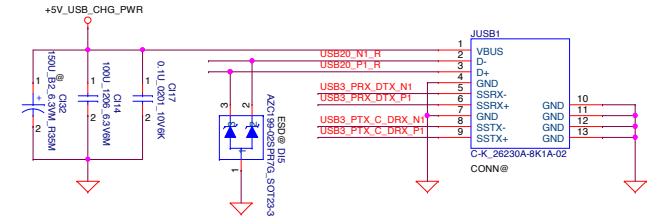
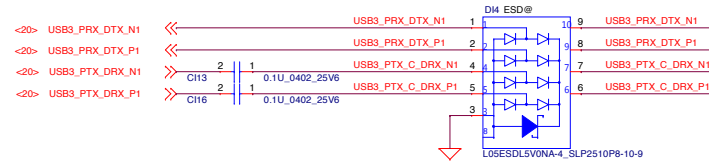
Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



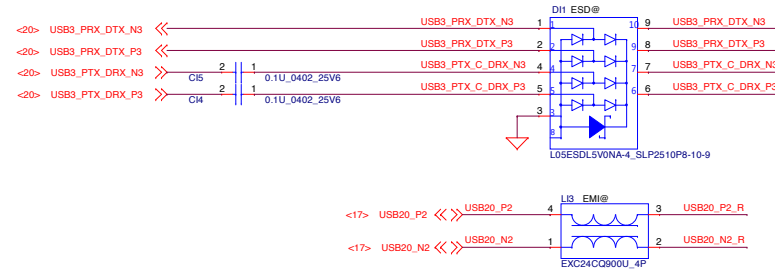
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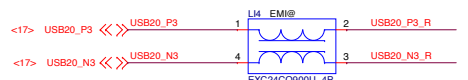
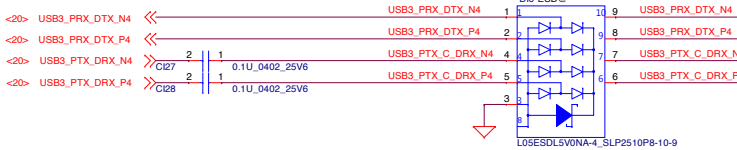
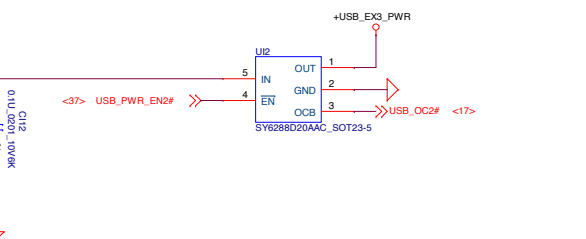
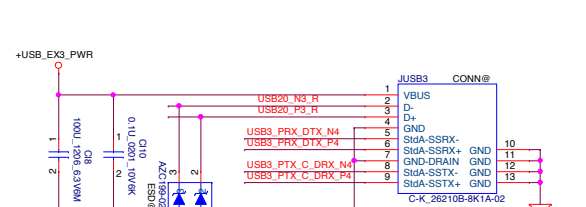
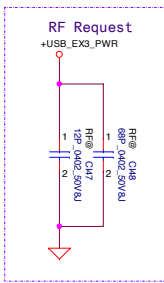
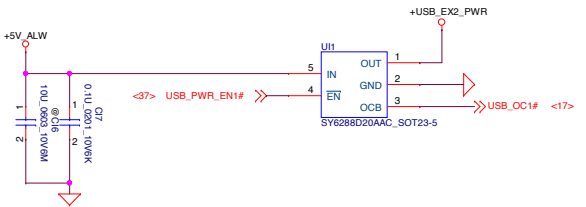
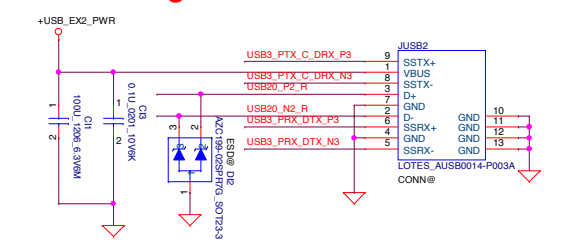
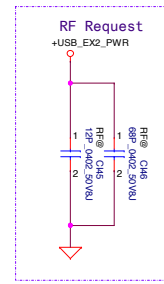
For PWR SW + Charger combine IC



# For Breckenridge 14&15/Steamboat 14



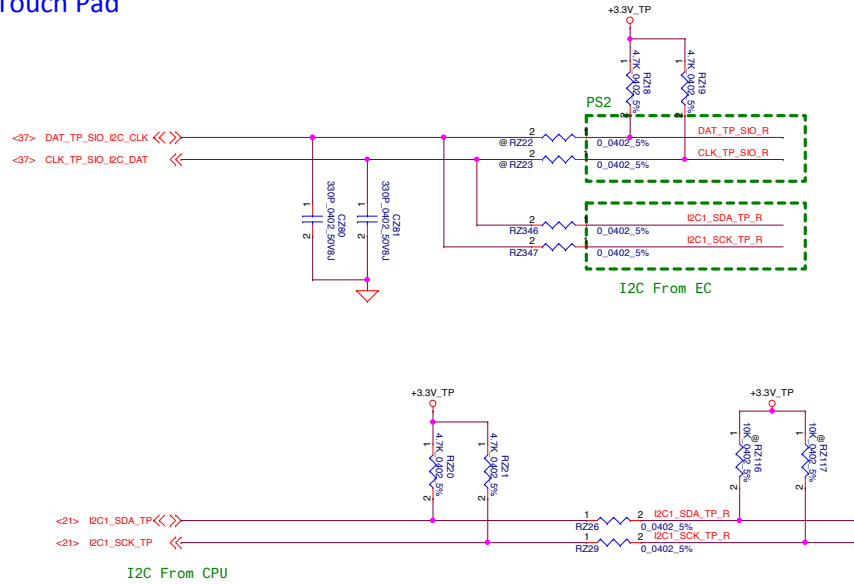
DfB request:  
main SM070003Z00 (INPAQ\_MCM1012B900F06BP\_4P)  
Footprint use 2nd source SM070004400 (PANAS\_EXC24CQ900U\_4P)  
Pitch change from 0.5mm to 0.55mm



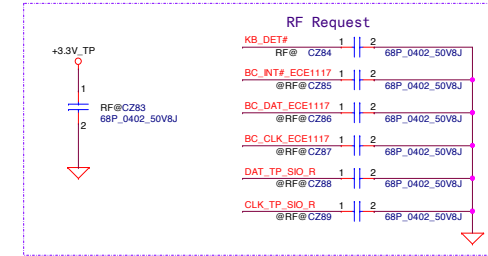
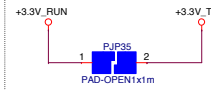
Security Classification		Compal Secret Data		ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED	
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		2017/01/01		Title	
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				JUSB2&JUSB3	
		Size		Document Number	
		LA-E141P		Rev	
				0.2	
		Date:		Wednesday, June 29, 2016	
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USB2&USB3

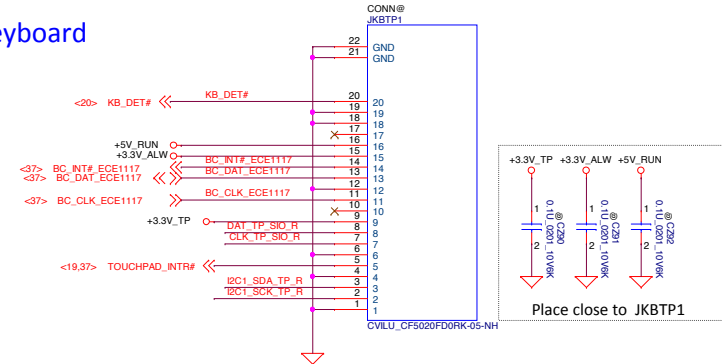
## Touch Pad



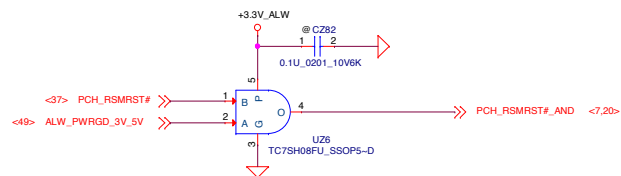
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)  
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows  
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



## Keyboard



## RSMRST circuit



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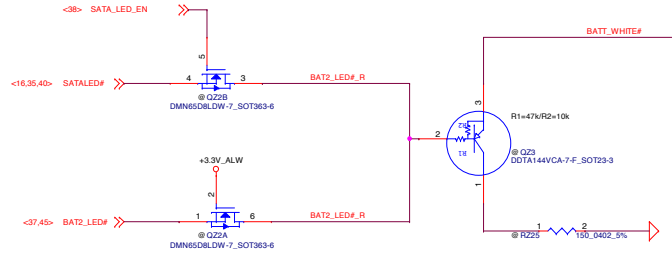
Compal Electronics, Inc.

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Date: Wednesday, June 29, 2016		Sheet 44 of 61			



## HDD LED MUX

means EC can switch battery white led and HDD LED by hot key "Fn+H"

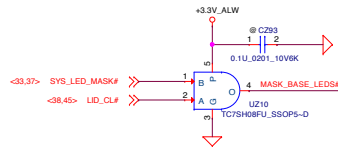
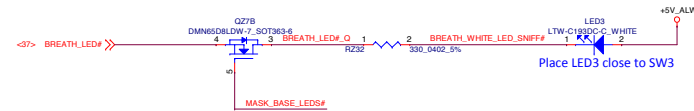


## Battery LED

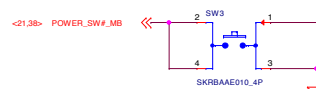


## Breath LED

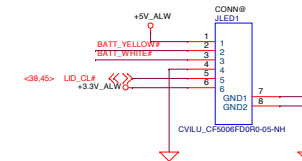
LED PIN change to SC50000FL00 from SC50000BA00



## POWER & INSTANT ON SWITCH



## LED board CONN

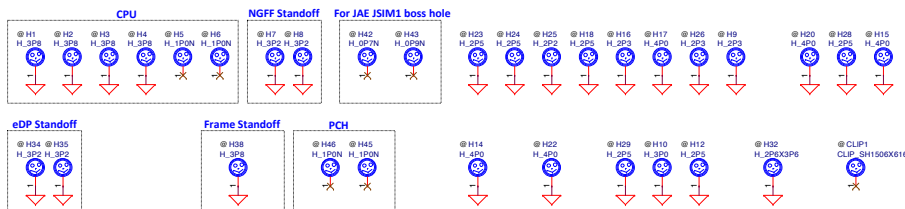


## Fiducial Mark



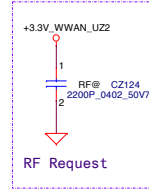
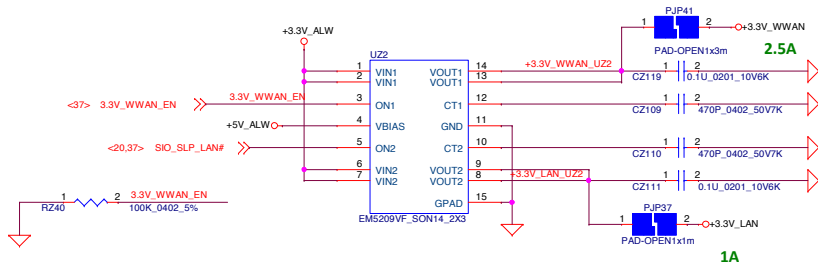
## LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

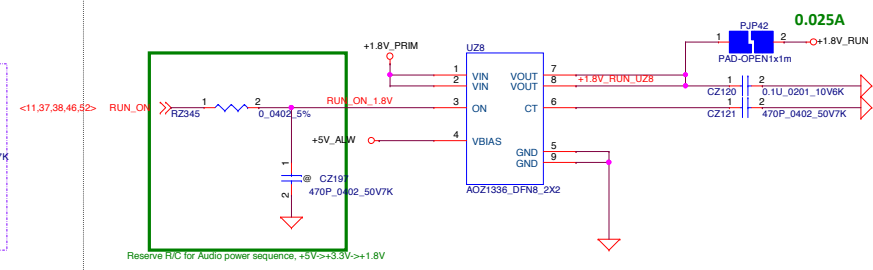


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Size C	Document Number LA-E141P	Date: Wednesday, June 29, 2016	Sheet 45 of 61

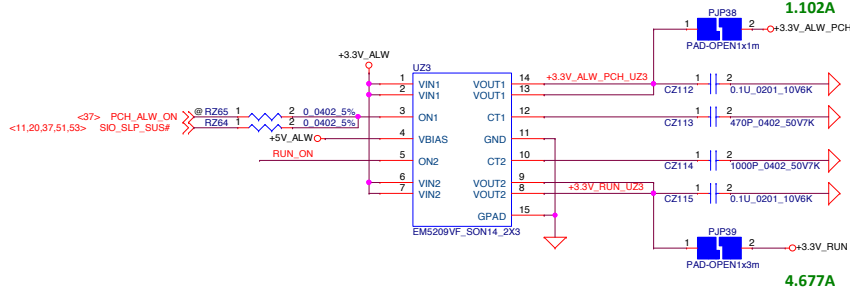
### +3.3V\_WWAN/+3.3V\_LAN source



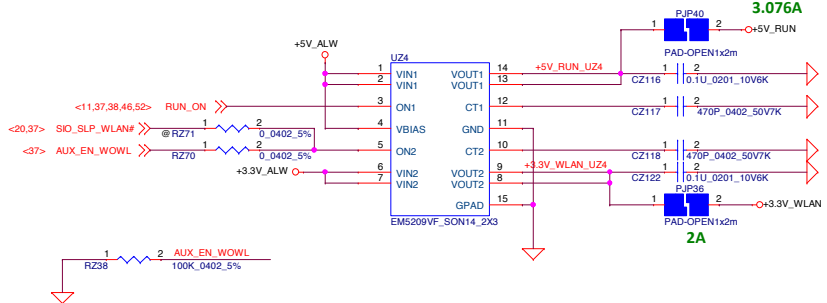
### +1.8V\_RUN source



### +3.3V\_ALW\_PCH/+3.3V\_RUN source

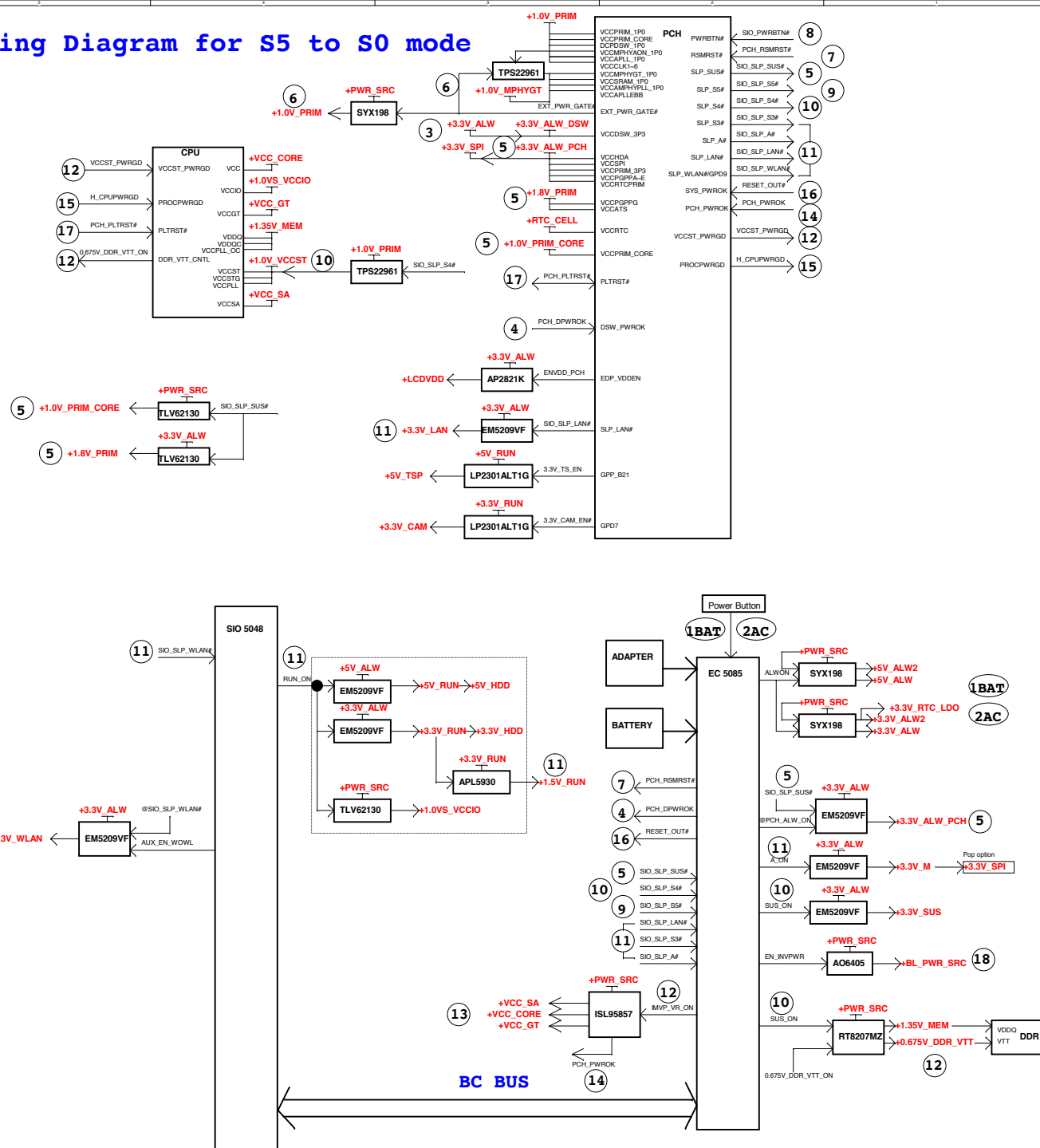


### +5V\_RUN/+3.3V\_WLAN source



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Size		Document Number		Rev		0.2	
B		LA-E141P					
Date: Wednesday, June 29, 2016				Sheet		46 of 61	

### Timing Diagram for S5 to S0 mode



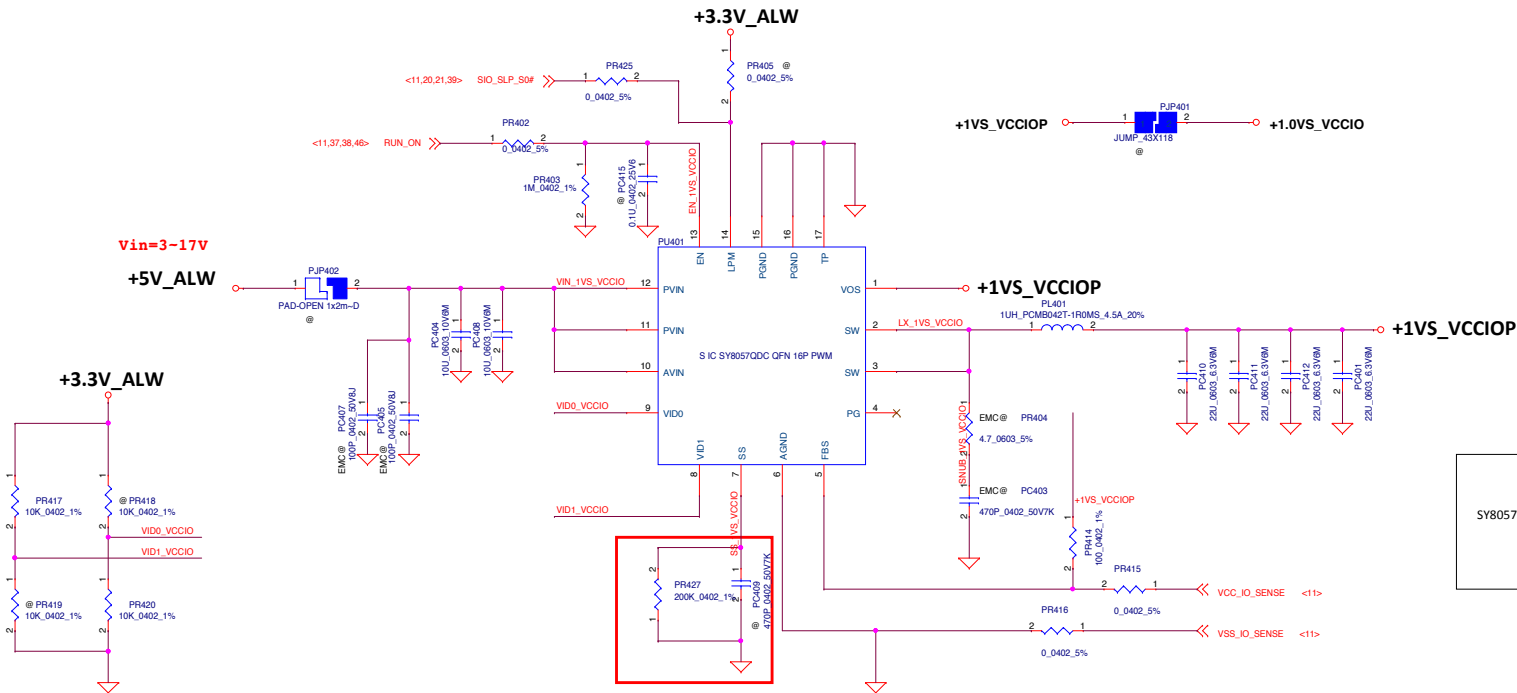
Security Classification	Compul Secret Data		DELL CONFIDENTIAL/PROPRIETARY <b>Compul Electronics, Inc.</b> <b>Power Sequence</b>
Issued Date	2016/01/01	Deciphered Date 2017/01/01	
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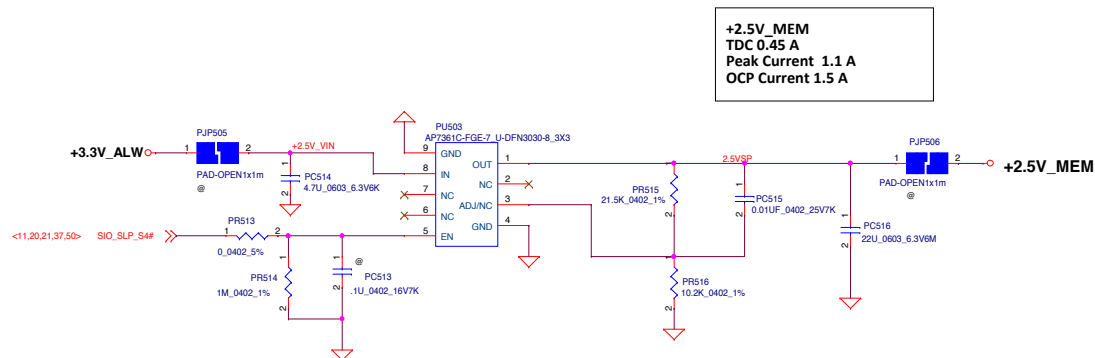
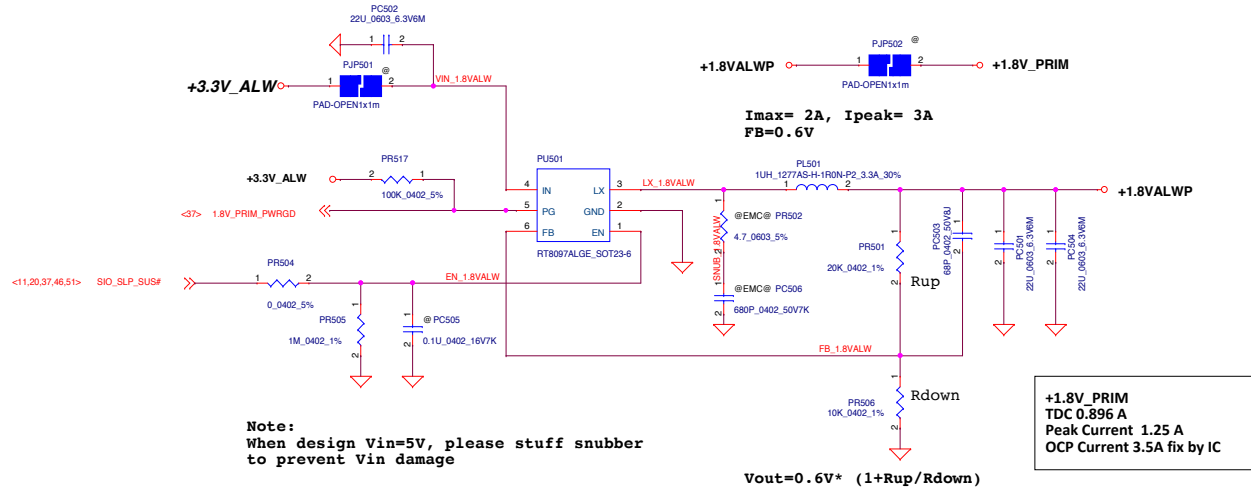


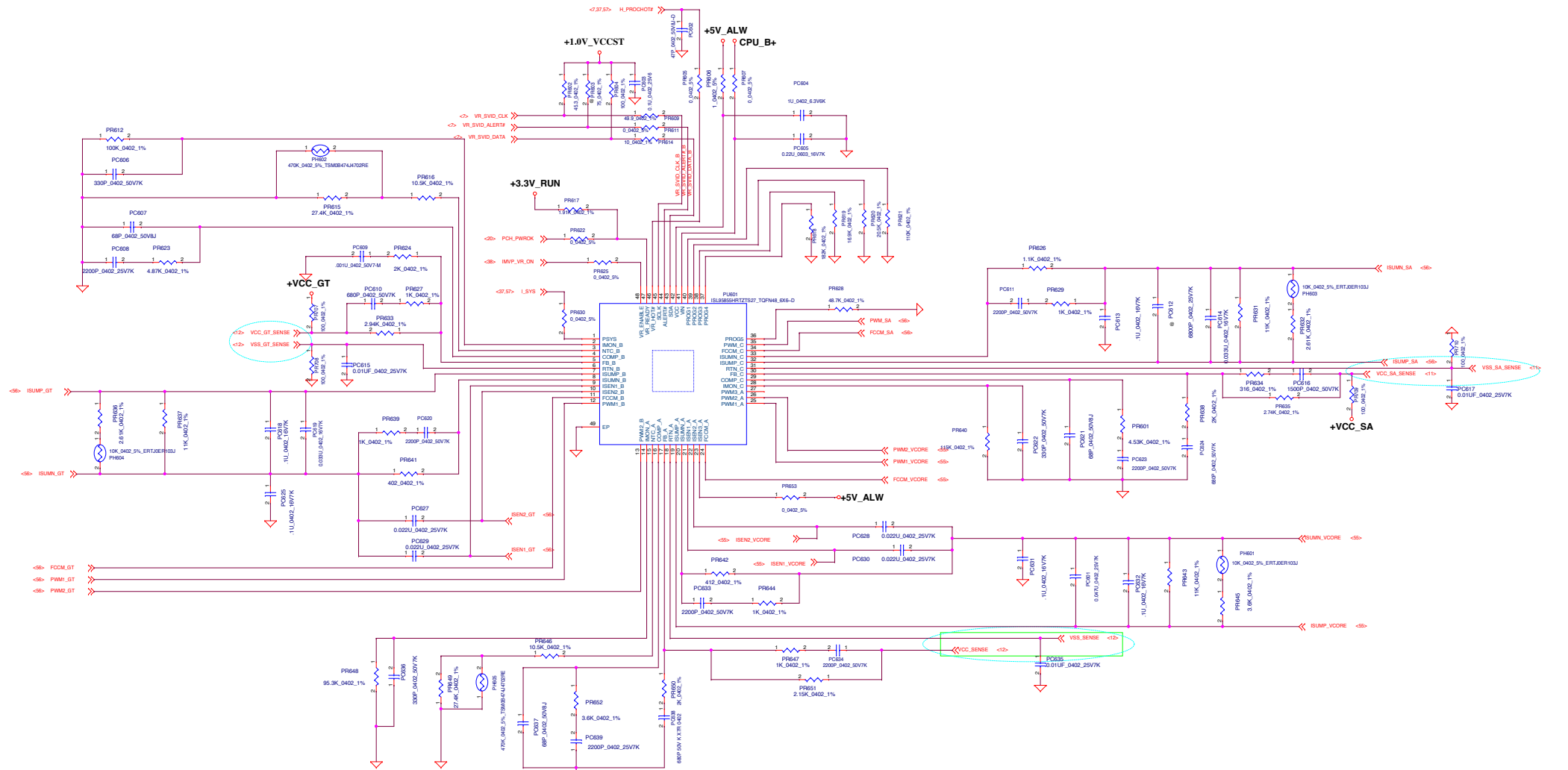
**+1.0VS\_VCCIO**  
TDC 3.9A  
Peak Current 5.5 A  
OCP Current 6.6 A Fix by IC  
TYP MAX

	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
SY8057	0	X	X	0(LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

Preset the different pull down resistor to choose the required power rail  
(VCCIO/PCH/EDRAM/EOPIO applications.)  
RMODE>500k or floating Vcc\_PRIM\_CORE.  
RMODE=200k Vcc\_IO.  
RMODE=0 Vcc\_EDRAM.







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Title		VCORE ISL95855	
Revision		1.0	
Date		Wednesday, June 29, 2016	

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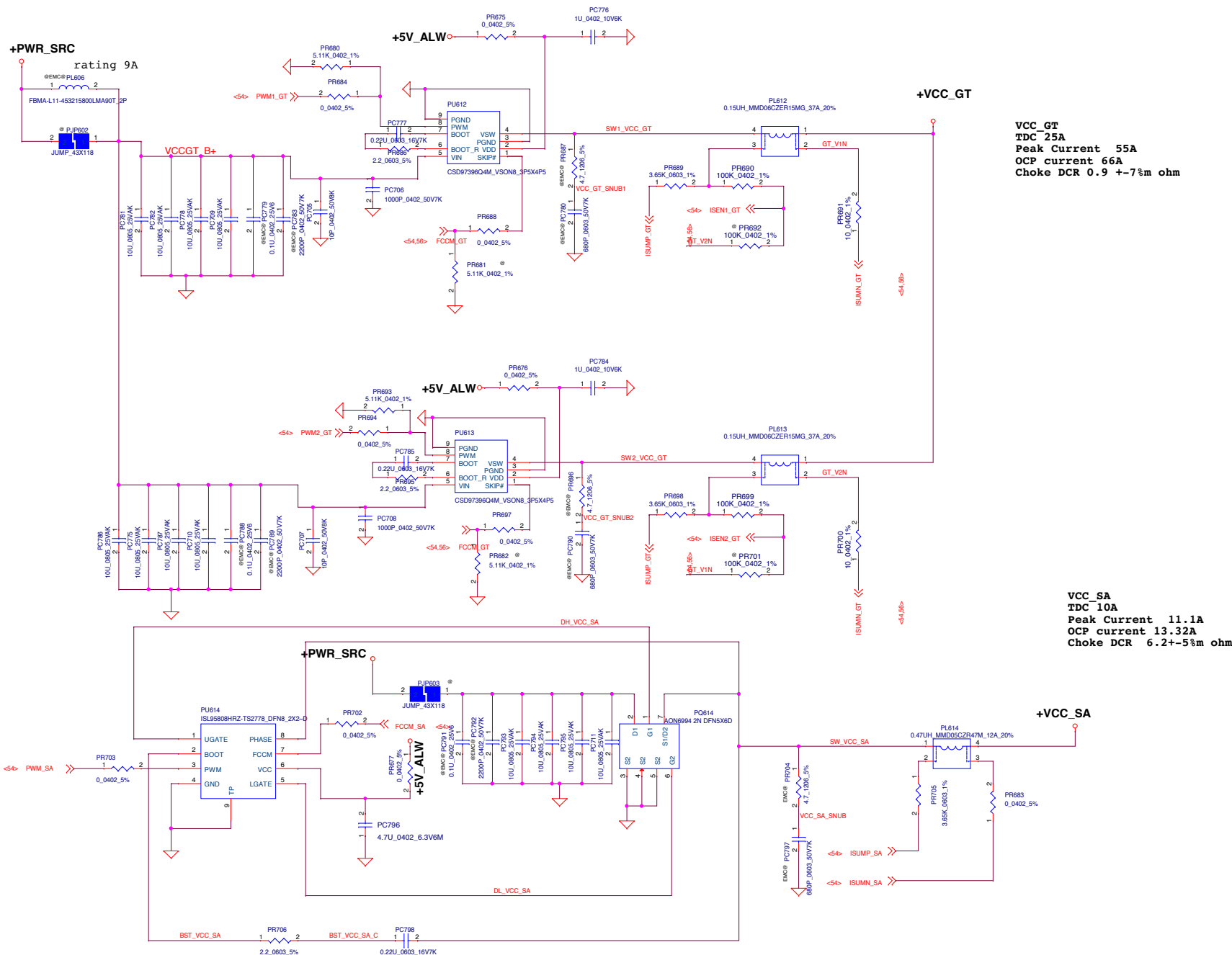
VCORE ISL95855

Document Number

LA-E141P

Page 02

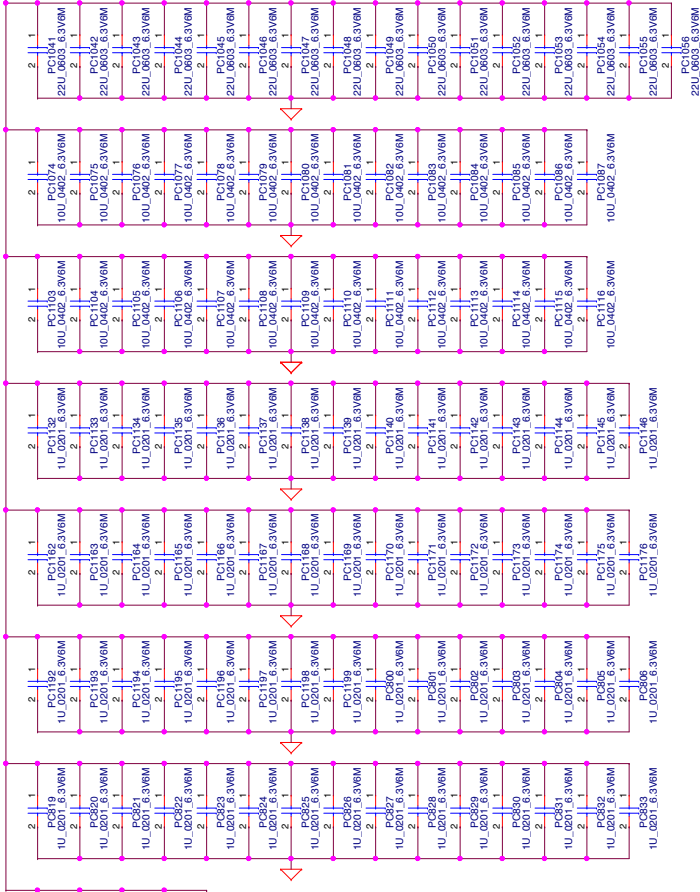






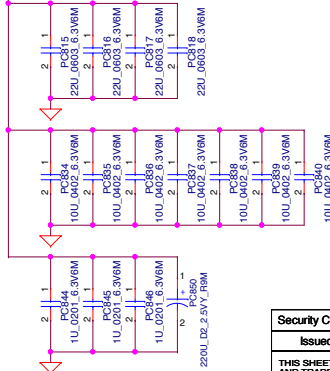
VCC\_CORE Place on CPU  
Back Side.  
22U\_0603 \* 8 pcs + 10U\_0402\*28 pcs + 1U\_0201\*35 pcs  
Primary Side.  
22U\_0603 \* 8 pcs+330u\_D2\*2 pcs

+VCC\_CORE



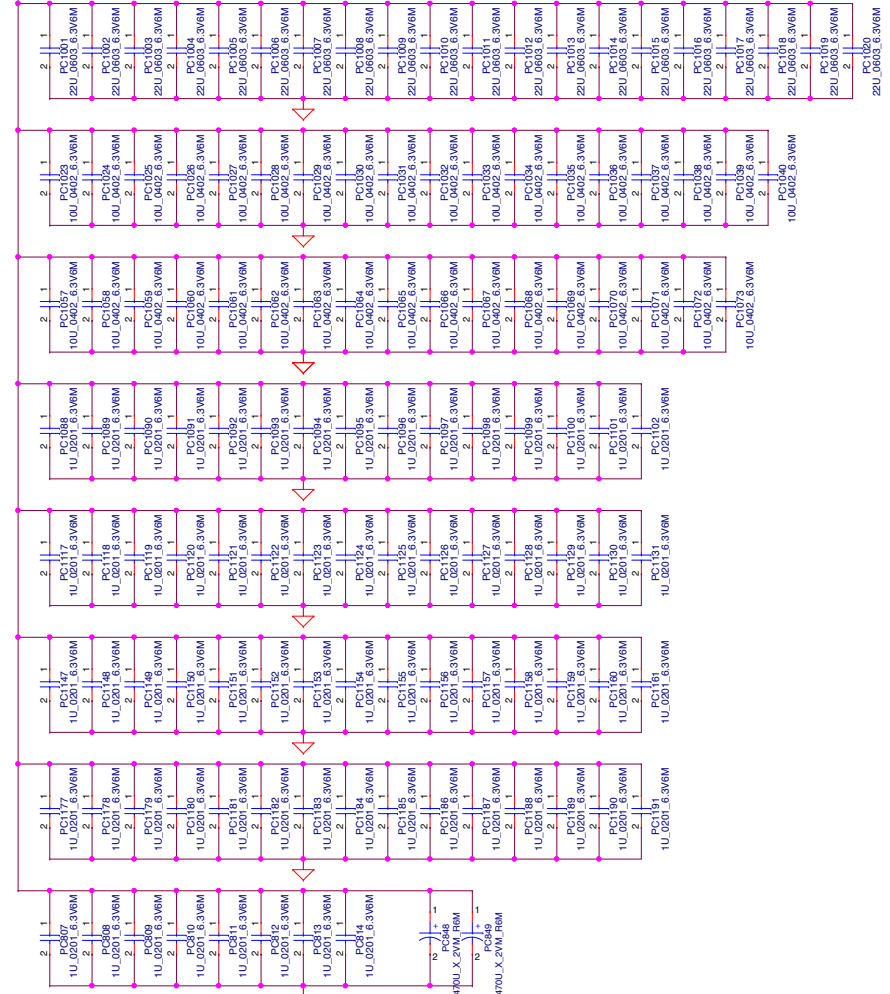
VCC\_SA Place on CPU  
Back Side.  
22U\_0603 \* 2 pcs + 10U\_0402\*7 pcs + 1U\_0201\*3 pcs  
Primary Side.  
22U\_0603 \* 2 pcs + 220u\_D2\*1 pcs

+VCC\_SA



VCC\_GT Place on CPU  
Back Side.  
22U\_0603 \* 8 pcs +10U\_0402\*35 pcs +1U\_0201\*68 pcs  
Primary Side.  
22U\_0603 \* 12 pcs +470u\_D2\*2 pcs

+VCC\_GT



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

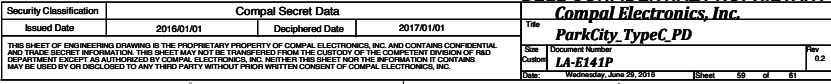
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PROCESSOR DECOUPLING

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					BELL COMMUNICATIONS CORPORATION	
INVESTMENT IN SUBSIDIARIES					FURNACE TECHNOLOGY INC.	
	AMOUNT	COST	FAIR VALUE	GAAP		FWD P/LR
[REDACTED]						
[REDACTED]						



Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	HW	2016/5/27	COMPAL	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
2	37	HW	2016/5/27	COMPAL	Reserve PORT80_DET# PD resistance	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
3	35	HW	2016/6/1	COMPAL	Intel schematics reivew modify item	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(0)_0201 to 10uF_0603	0.2(X01)
4	39	HW	2016/6/1	COMPAL	TPM change to NUVOTON	Change TPM from Atmel to NUVOTON.	0.2(X01)
5	35	HW	2016/6/1	COMPAL	Intel reviw result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
6	35	HW	2016/6/7	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
7	37	HW	2016/6/7	COMPAL	For MEC5105K-D1-TN setting	1. Change UE1 to SA00009GL00 2. POP RE360,RE362 3. De-POP RE361	0.2(X01)
8	35,32	HW	2016/6/16	COMPAL	For EMC request	De-pop RZ131, RZ132. CL22 change to 10pf , POP CA7,CZ1 (100P),CH268 modify from 22p to 47p and POP,Change LV1 to SM01000NY00	0.2(X01)
9	41	HW	2016/6/16	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	POP RN5	0.2(X01)
10	39	ME	2016/6/17	COMPAL	Connector change	1. JKBTP1 change to CVILU_CF5020FDORK-05-NH 2. JUSH1 change to CVILU_CF5026FDORK-05-NH 3. JIR1 change to ACES_50208-0060N-P01	0.2(X01)
11	36	HW	2016/6/20	COMPAL	Vender suggest	RA7,RA8 change to 16.2ohm	0.2(X01)
12	37	HW	2016/6/22	COMPAL	The posibility of GPIO map update	Add RE514,RE515 for RTCRST_ON	0.2(X01)
13	41	HW	2016/6/22	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)